INVESTIGATION OF INTERFACE STATES AND FAILURE MECHANISMS IN MNOS DEVICES

By

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The objective of this dissertation is to conduct a quantitative study of the interface state characteristics at $Si-SiO_2$ interface and the failure mechanisms in the silicon MNOS nonvolatile memory devices under different write/erase (W/E) cycling conditions. The main thrust of this research is to quantitatively characterize the interface states in MNOS devices and to correlate the results of the measurements to the failure mechanisms in the exercised MNOS devices for W/E cycles up to $1x10^{11}$ cycles. The Constant-Capacitance Deep Level Transient Spectroscopy (CC-DLTS) technique is employed for the first time to characterize the interface states in the MNOS device. The existing theory for the CC-DLTS technique is modified to analyze the interface state density and

electron capture cross sections of the trap states at Si-SiO_2 interface. An exact equivalent circuit model for the P^+-gridded MNOS capacitors is developed to predict the high frequency C-V behavior in the exercised MNOS devices. The results show little change in the interface state density was observed for W/E cycles less than $1x10^7$ and increased rapidly for W/E cycles greater than $1x10^7$. For W/E cycles greater than $5x10^9$, a gradual increase in interface state density with W/E cyclings was observed.

The negative shift of threshold voltage in the exercised MNOS devices can be attributed to the creation of interface states for W/E cycles less than 10^9 and primarily due to the generation of interface states for W/E cycles exceeding $1x10^9$. The increase in interface state densities and the degradation of the thin oxide layer after prolonged W/E cycling increase the back tunneling current which results in the increase of retention decay rate. Furthermore, mobility degradation in the inversion layer was observed in the MNOS transistors for W/E cycling exceeds 10^9. This is attributed to the generation of surface state densities. Improvement in retention and endurance of the MNOS transistors may be achieved by altering NH_3/SiH_4 ratio, oxide thickness and annealing conditions. The scale-down Metal-Oxide-Nitride-Oxide-Silicon (MONOS) structure may enhance the performance of MNOS nonvolatile memory devices.

CHAPTER I
INTRODUCTION

It is well known that interface states at the silicon-oxide ($Si-SiO_2$) and oxide-nitride ($SiO_2-Si_3N_4$) as well as trap states in the nitride film play an important role in influencing the performance of MNOS devices. However, the physical mechanisms underlying charge transport, charge storage, and device failure mechanisms are not yet well understood. In order to improve the device performance and to optimize the fabrication process, it is essential that we gain a better understanding of the physical properties of interface states and deep level traps within the energy bandgap of the MNOS device. In addition, it is also important to determine the correlation between the interface states and the failure mechanisms in the exercised MNOS devices. Earlier studies have shown that charge retention and endurance are directly related to the interface states at $Si-SiO_2$ interface and trap states in the nitride.

It is believed that repeated write/erase (W/E) cyclings of an MNOS device will alter the physical properties of interface states, and prolonged operation (e.g., W/E cycle exceeding 10^{11}) will result in the total

failure of the device. In fact, we have observed a significant increase in the interface states density at the Si-oxide interface for W/E cycles exceeding 10^9 on Harris's MNOS devices.

The two most important degradation effects in MNOS memory transistors are a negative shift of the threshold voltage and a loss of the retention time. The negative shift of threshold voltage was predicted as a result of the creation of new surface states at $Si-SiO_2$ interface. As to the retention loss, it was also ascribed to the increase in surface state density. The increase of the retention decay rate after prolonged cycling was suggested as due to the increased back tunneling current from nitride-oxide interface via thin oxide layer into silicon conduction band. Unfortunately, little work has been reported concerning the relationship between the interface states and the endurance and retention characteristics in the MNOS devices.

The thin oxide layer in an MNOS device is to overcome the unstable behavior observed in a nonvolatile MNS device. The degradation or break down of the thin oxide layer may be responsible for the failure in the MNOS device. The main objective of this dissertation is to investigate the properties of the thin oxide layer and the change of interface states relating to the memory operation of MNOS devices in a quantitative manner.

Several experimental methods for characterizing the interface states at the silicon-oxide and oxide-nitride interfaces of an MNOS device have been reported previously. The combined quasi-static capacitance-voltage (QSCV) and high frequency capacitance voltage techniques (HFCV) are the most commonly used methods for characterizing the interface states at the $Si-SiO_2$ interface of MOS and MNOS devices. However, there are drawbacks in the QSCV technique for interface state characterization in the MNOS device as will be discussed later. The Deep Level Transient Spectroscopy (DLTS) and the Constant Capacitance DLTS (CC-DLTS) techniques have been recently used by several researchers for determining the bulk traps, the interface state density and the capture cross section in MOS devices. Nevertheless, none has been reported in the literature concerning the use of the CC-DLTS technique for interface state characterization in the MNOS device.

The objective of this research is to investigate the effects of interface states at $Si-SiO_2$ interface on the MNOS device degradation under different exercised conditions. The CC-DLTS technique is applied to investigate the $Si-SiO_2$ interface state characteristics. The P^+-gridded MNOS capacitor structure is used for the CC-DLTS measurements for different W/E cyclings. An exact equivalent circuit model for a P^+-gridded MNOS capacitor is developed to predict the high frequency C-V behavior in the exercised MNOS capacitors.

An overview of the MNOS research is given in Chapter II. The basic theory of an MNOS memory device is presented in Chapter III, in which the degradation phenomena such as the reduction in endurance and the retention loss are discussed, based on the results reported by Harris.

In Chapter IV, the existing theory for the CC-DLTS technique is modified for surface state measurements on P^+-gridded MNOS devices. The CC-DLTS technique is a powerful tool for study the dynamic properties of interface states at $Si-SiO_2$ interface. Surface state densities, trap energy distribution, and electron capture cross sections in the upper half bandgap of silicon are determined by this technique.

Chapter V presents the CC-DLTS experimental set up and discusses the results of $Si-SiO_2$ interface states measurements on different device structures and usder different exercised conditions. The effects of W/E pulse amplitude and pulse duration on surface states are also examined. The generation of surface state density after prolonged W/E cycling (up to 10^{11} cycles) is discussed.

The analysis of high frequency capacitance-voltage measurements for a P^+-gridded MNOS capacitor structure provides a detailed view on the device degradation mechanism; this is presented in Chapter VI. A quantitative interpretation of the threshold voltage shift and the mobility reduction in the inversion layer of MNOS capacitors after prolonged W/E cyclings is also given in Chapter VI.

A summary and the main conclusions of this dissertation are given in Chapter VII. Suggestions for future research are also included.

CHAPTER II
OVERVIEW

In this chapter the state of the art in the study of MNOS devices is reviewed. Extensive investigation has been reported on MNOS devices in the literature concerning the charge trapping mechanisms at the Si-oxide and Oxide-nitride interfaces as well as in the bulk trap states of the nitride layer. In an effort to obtain a better understanding of the basic mechanisms and to correlate the interface states and traps in the nitride to the failure mechanisms in the MNOS device, several diagnostic tools have been developed in the past decade. Although progress has been made in this area, understanding of the interface state characteristics and the bulk traps in the MNOS devices are still far from satisfaction. Lack of quantitative correlation between the interface trap parameters and the performance parameters of the MNOS device has hindered the progress in the MNOS technology. In the following, we review the work which has been published in the literature concering the interface state properties at the Si-oxide and Oxide-nitride interfaces as well as bulk traps in the nitride layer of the MNOS device.

It is well known that various degradation phenomena such as negative shift and decrease of threshold

window, a decrease in the channel conductance and the retention time occur with the increasing number of write/erase cycles[1-4]. Several investigators have found that frequent W/E cycles or d.c stress would introduce a significant increase in the density of the Si-oxide interface states[5].

Suzuki and Hayzski [6,7] proposed that the MNOS device degradation was directly related to the increase in surface state density. Maes et al.[8] introduced the thermal annealing method to eliminate the back tunneling of holes to Si-oxide interface states. Popova et al.[9] suggested that the surface states affected the write state due to the filled traps at the Si-oxide interface. Schuermeyer and Young [10] and other researchers [11-12] have found that memory decay ascribed to the increase of surface state density after extended W/E cycling. White et al. [13] and White and Chricci [14] have shown that the short term cycling decay is mainly due to the influence of interface states. Huang [15] has attributed to the generation of surface states by the emission of minority carriers. Jeppson and Svensson [3] reported that the negative shift of the threshold voltage is caused by a strong increase of the density of Si-oxide interface states.

In an effort to study the effect of interface state traps at the Si-oxide interface on the endurance and memory retention of an MNOS device, several experimental techniques have been reported in the past. These include the

quasi-static capacitance-voltage (QSCV) and the high frequency capacitance voltage (HFCV) techniques [16-19], the charge-pumping method [20], the thermal-dielectric-relaxation-current (IDRC) technique [21-22], the deep level transient spectroscopy (DLTS) technique [23]. The surface state densities reported by Sinah and Simmons [16], Tutto and Balazs [17], Popova et al. [18], Helms et al. [19] using the QSCV technique on an MNOS structure were found in the range of 10^{10} to 10^{12} $eV^{-1}cm^{-2}$. These results are in good agreement with our interface state density data determined by the CCDLTS technique to be discussed in chapter IV. Uranwala et al.[22] used the TDRC and IDRC techniques to obtain the energy distribution of interface state traps situated throughout the bandgap of an MNOS device. They observed two main peaks with energy of E_c-0.40 eV and E_c- 0.74 eV for the interface trap states. Our CCDLTS data revealed that the peak interface state was located near the E_c-0.37 eV. The conventional DLTS technique has also been employed by several researchers [24-26] to study the interface state density and energy distribution in the MOS structure. Values of the interface state densities determined by this method were found in the range of high 10^{9} to low 10^{11} $eV^{-1}cm^{-2}$.

Investigation of the charge centroid in the nitride layer has been widely discussed in the literature for predicting the behavior of memory charges in the bulk nitride layer and at the oxide-nitride boundary;

techniques which have been used include the Yun's method [27], the staircase method [28] by Lehovec et al. and others [29-33]. The average trap density measured in the nitride film was in the range from mid $1x10^{17}$ to low $1x10^{19}$ cm^{-3}. Kapoor, Delatore, and Turi [34-35] used the internal photoelectric effect technique along with high frequency capacitance voltage method to study the nitride film properties. From conductance measurements, Endo [36] has reported a donor-like electron trap in the bulk nitride film with a density of about $4x10^{17}$ cm^{-3}. Katsube et al. [37] have reported the use of TDRC and IDRC techniques to measure trap capture cross section (with a value of $5x10^{-13}$ cm^2) and the energy distribution of bulk traps in the nitride layer. The results of these studies show that memory traps are distributed 50 Å deep into the nitride with several trap levels below the conduction band edge of the nitride; the charging and discharging mechanisms are due to the cascade connection of tunneling and thermal excitation of trap states in the nitride. The trap density at the oxide-nitride interface is in the range of $1x10^{10}$ to $1x10^{13}$ eV^{-1}-cm^{-2}.

The above discussion provides a general overview of the work that has been reported in the literature concerning the state of the art knowledge of the interface state characteristics at the Si-oxide and oxide-nitride interfaces as well as traps in the nitride layer of an MNOS device.

CHAPTER III
FUNDAMENTAL CHARACTERISTICS OF AN MNOS MEMORY DEVICE

3.1 Physical Structure

A cross section view of a P-channel MNOS transistor is shown in Figure 3.1. The structure resembles a conventional MOS field-effect transistor in which the thermal oxide is replaced by a double dielectric layer in the gate area. The gate dielectric consists of a thin layer (20 Å) of nature oxide (SiO_2) over which a layer of silicon nitride (200-800 Å) is deposited. The MNOS devices used in this study were processed on <100> silicon wafers using LPCVD nitride of 465 Å thickness deposited at 750 C over a 20 Å thin nature oxide layer on N-silicon substrate.

The thick nitride layer gives the low ion drift and radiation-hard properties. The thin oxide layer is used to prevent the unstable behavior of charge accumulated at the silicon nitride-silicon interface in the MNS structure. Above a critical bias voltage, it exhibits hysteresis behavior of turn-on voltage as a function of applied gate voltage, resulting from stable charge storage at the silicon nitride-silicon dioxide interface.

Figure 3.2 is an ideal energy band diagram for an MNOS

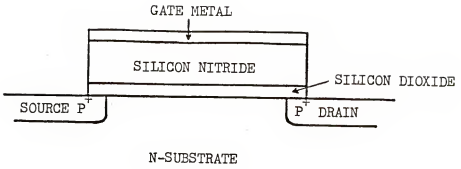


Figure 3.1 A cross section of a P-channel MNOS transistor

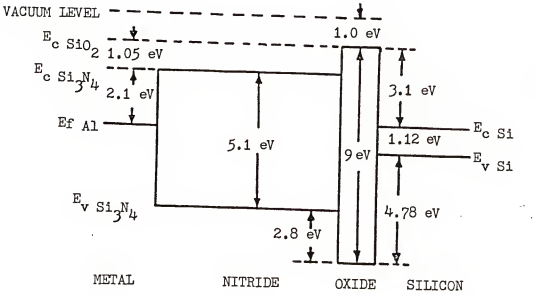


Figure 3.2 Energy-band diagram of the Al-Si_3N_4-SiO_2-Si MNOS capacitor structure

structure. When an appropriate polarity and sufficiently high voltage is applied to the gate, carriers will be accumulated in the region of oxide-nitride interface due to the difference in conductivity in these two insulating layers. Figure 3.3 shows the energy band diagram and the corresponding C-V curves and the threshold voltages for an MNOS capacitor. Figure 3.3(a) shows the condition of a positive charge accumulation at the oxide-nitride interface. Figure 3.3(b) shows the condition of a negative charge accumulation at the oxide-nitride interface, and Figure 3.3(c) shows the C-V curves and the threshold voltage of an MNOS transistor.

The storage function associated with the hysteresis characteristic leads to the potential application of variable turn-on voltage MNOS transistors in random-access and alterable read-only semiconductor memories as well as digital circuit switch nonvolatile storage capability.

3.2 Carrier Transport in SiO_2 and Si_3N_4 Insulating Films

To study the charging and discharging behavior of an MNOS device, several models and theories have been reported. [38]. The one dimensional continuity equation used to calculate the transient behavior of an MNOS device is givien by

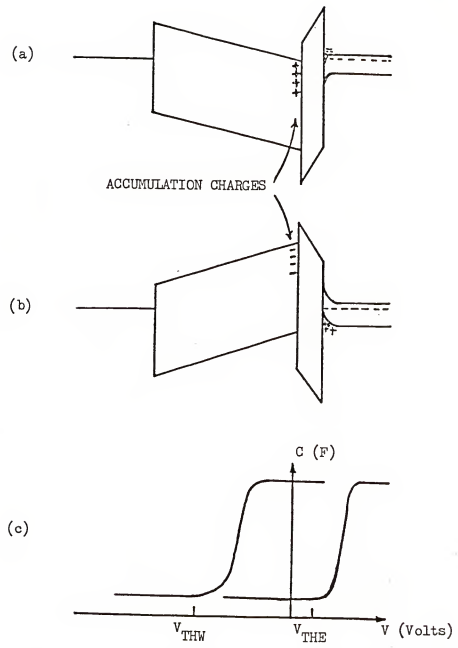


Figure 3.3 The energy band diagrams and CV plots after write/erase exercises (a) the zero bias condition after "write" programming, (b) the zero bias condition after "erase" programming, (c) the corresponding CV curves and the threshold voltages at "write" and "erase" memory states

$$\frac{\partial J_x}{\partial x} + \frac{\partial \rho}{\partial t} = 0 \qquad (3.1)$$

where J_x is the conduction current density in the x direction, defined as being perpendicular to the gate insulator layer, and ρ is the volume charge density. It has been suggested [38] that the charge is trapped only at the oxide-nitride interface, not in the bulk of nitride layer. Thus, the conduction current density becomes spatially independent in the nitride and oxide layers, and may be represented as J_o in the SiO_2 layer and J_n in the Si_3N_4 layer. After a gate voltage is applied, J_o, J_n, and the interface charge Q_I (per unit area) are all functions of time t. Then Equation (3.1) becomes

$$\frac{d\, Q_I(V_g,t)}{dt} = J_o(V_g,t) - J_n(V_g,t) \qquad (3.2)$$

Equation (3.2) was used to numerically calculate the switching and charge-retention characteristics.

For a Si-SiO_2 system the electric field for silicon at breakdown is about $3x10^5$ V/cm [39], while the corresponding field in the oxide layer is three times larger (Si/ SiO_2=11.7/3.9), that is, about 10^6 V/cm. For an ultra-thin SiO_2 layer, or under a very high electric field, tunneling will occur, which may lead to a much larger oxide conduction current as compared to the nitride conduction current. The related carrier-injection mechanism

and conditions are summarized as follows:

a) The Fowler-Nordheim Tunneling, as is shown in Figure 3.4, is proposed [40-41] for a thick (> 50 Å) oxide MNOS device in which electrons emit from the silicon conduction band into the oxide conduction band drift into the nitride conduction band and then trap in nitride traps under very high electric field. The tunneling current is strongly field-dependent

$$J_o = C_{FN} E^2 \exp(-\frac{E_o}{E_{ox}}) \tag{3.3}$$

where E_o and C_{FN} are characteristic constants, E_{ox} is electric field across oxide layer.

b) The Direct tunneling of electrons from the silicon conduction band through the oxide into traps in the nitride band gap as shown in Figure 3.5. All the direct tunneling models assumed only electron tunneling [42-47]. The current depends on the oxide field strength, the initial and final density of nitride traps, barrier height under Write/Erase exercise, the vibration or attempt to escape frequency of the charge in the traps, and the oxide thickness. White et al. [48] presented an expression for the oxide tunneling current which included the $Si-SiO_2$ interface state density as

$$J_o = a Q_I N_{st} \exp(-bx_{ot}) \tag{3.4}$$

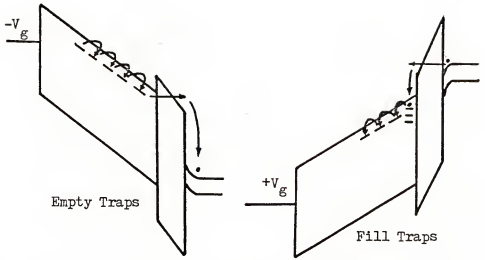


Figure 3.4 Fowler-Nordheim emission of electrons into the Oxide conduction band during carrier switching in an MNOS structure

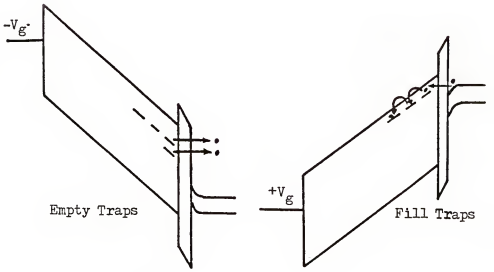


Figure 3.5 Direct tunneling of electrons through thin Oxide layer between monoenergetic traps in nitride and silicon conduction band of an MNOS structure

where a and b are constants, N_{st} is the Si-SiO_2 interface state density and x_{ot} is an effective tunneling distance for the centroid of the stored charge.

c) Modified Fowler-Nordheim tunneling model was extended to thin oxide (<50Å) devices in which electrons were assumed to tunneling from the silicon conduction band through a portion of the nitride layer into traps under positive gate bias as shown in Figure 3.6. The trapped charge is removed under negative gate bias via two phenomena: (1) direct tunneling of electrons from the traps in the nitride into the silicon conduction band and (2) tunneling of holes from the silicon valence band into the nitride valence band, followed by hole trapping and trapped electron-injected hole recombination. The oxide conduction current was given by Lundstrom and Svensson [46] as

$$J_o = C_{fn} E_{ox}^2 P_{ox} P_n \tag{3.5}$$

where C_{fn} is a constant characteristics of Fowler-Nordheim tunneling from silicon into slicon-dioxide and E_{ox} is the magnitude of the electric field in the oxide; P_{ox} and P_n are the transmission probabilities through the oxide and nitride, respectively.

d) Trap assisted charge injection under a low field condition is proposed by Lundstrom and Svensson [49]. The electron (or hole, for the opposite polarity) injection from the silicon conduction (valence) band via a trap as an

intermediate state is shown in Figure 3.7. The tunneling current to the trap level can be written as [50]

$$J_o = q\, P_o N_t \int_{T_{ox}}^{x_t} [1 + \exp(\frac{q(V-V_f)}{kT})]^{-1} P_{ox} P_n dx \qquad (3.6)$$

where x_t is the distance of traps from the $Si-SiO_2$ interface, P_o is a constant, N_t is the density of traps in the nitride, and V_F is the Fermi potential in the silicon.

The current through the nitride consists of three components: an Ohmic current at low nitride fields, a Poole-Frenkel type current at intermediate fields, and an additional component due to the charge-hopping mechanism at high fields [41]. Thus, the total current in the nitride is given by

$$J_n = J_{n1} + J_{n2} + J_{n3}$$

where J_{n1} in the current density due to hopping of thermally excited electrons between isolated trapping states, and can be written as

$$J_{n1} = C_1 E_n(V_g,t)\, \exp(-q\phi_1/kT) \qquad (3.7)$$

where E_n is the electric field in the nitride, $q\phi_1$ is the thermal activation energy; J_{n2} corresponds to field-enhanced thermal excitation (Poole-Frenkel effect) and is given by

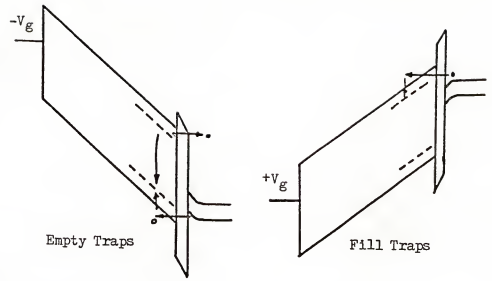


Figure 3.6 Modified Fowler-Nordheim tunneling into the nitride conduction band in an MNOS structure

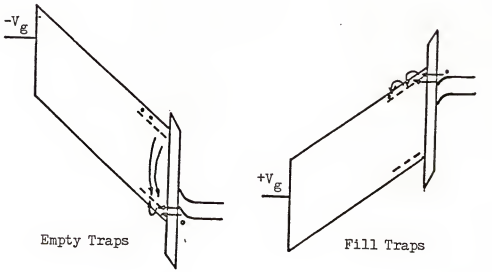


Figure 3.7 Trap-assisted tunneling through the oxide into the nitride of an MNOS structure

$$J_{n2} = C_2 E_n(V_g,t) \exp\left[-\frac{(q\phi_2 - \sqrt{q\, E_n(V_g,t)/\pi\, \epsilon_n})}{kT}\right] \qquad (3.8)$$

where ϕ_2 is the depth of the trap-potential well; C_1 is characteristic constant depending on the trap level and the dielectric constant; J_{n3} is due to the field emission of trapped electrons into the dielectric conduction band:

$$J_{n3} = C_3 E_n^2 (V_g,t) \exp\left(\frac{-E_{cc}}{E_n(V_g,t)}\right) \qquad (3.9)$$

where C_3 and E_{cc} are characteristic constants depending on the trap level.

The physical constants for the three current components in a silicon MNOS device are given by

$E_n = 7.5E_o$ permittivity of Si_3N_4

$\phi_1 = 0.1$ V

$\phi_2 = 1.0 \pm 0.2$ V

$E_{cc} = 1.2 \times 10^8$ V/cm

$C_1 = 5.0 \times 10^{-14}$ A/V cm

$C_2 = 3.0 \times 10^{-9}$ A/V cm

$C_3 = 3.5 \times 10^{-10}$ A/V^2

3.3 Endurance and Retention of an MNOS Memory Device

MNOS transistors have been employed in commercial and military applications, as electrically programmable,

nonvolatile semiconductor memory elements. The threshold voltage V_{th} of an MNOS transistor can be altered by applying a suitable pulse to the gate with respect to the drain, source, and substrate of the transistor. The amplitude of the gate-voltage pulse during the writing and erasing cycle is much larger than that of the reading state. For example, for a typical MNOS transistor, if a gate voltage pulse of +25 volts is applied to write and erase operation, it would result in an electric field in the oxide of more than 10^7 V/cm. It is well known that various degradation phenomena, e.g., a shift and decrease of the threshold window, a decrease in channel conductance, and a decrease in the retention time, occur with increasing numbers of W/E cycles. Therefore, an understanding of the degradation mechanism is very important for advancing the state of the art technology in these devices.

The C-V mesurement is one of the diagnostic tools being used to characterize the memory states. The P^+ gridded diffusion grids are used on N-type silicon substrates for the MNOS capacitors used in this study. It provides both the majority and minority carriers injection into the silicon-nitride layer. This allows the writing and erasing of a test capacitor with pulse lengths comparable to those used for programming MNOS transistors (on the order of microseconds). In turn, this programmability makes possible the endurance testing for the MNOS capacitor. A typical pulse C-V characterization

plot at 1MHz for a gridded capacitor is shown in Figure 3.8. The capacitor under test received no endurance exercising at the beginning. The diffused P-type grids in the substrate were connected electrically to the N-type substrate.

Figure 3.9 shows additional data on the same capacitor taken after exercising the device for 2.8×10^9 W/E cycles with one microsecond, 30 volts pulse. A considerable change in the C-V curve was noted due to exercising. All of the traces had shifted towards more positive flat-band voltages. The slope of the curve in the depletion stage of the characteristic curves diminished with exercising. Finally, the width of the "U" shape was greatly broadened after the W/E exercising.

A typical plot of endurance characterization curves for an exercised MNOS transistor is shown in Figure 3.10. The written and erased threshold voltages of the device being characterized were plotted as a function of the total number of write-erase cycles experienced by the device. The outer two curves were data taken 0.1 seconds after programming for measurement. The inner two curves were data taken 100 seconds after programming. The difference between the threshold voltage in write state, V_{thW}, and the threshold voltage in erase state, V_{thE}, is defined as "memory window". The magnitude of window determines the distinguish ability of memory logics. In this figure, device was exercised with $\pm$25 volts in amplitude and 1 μsec

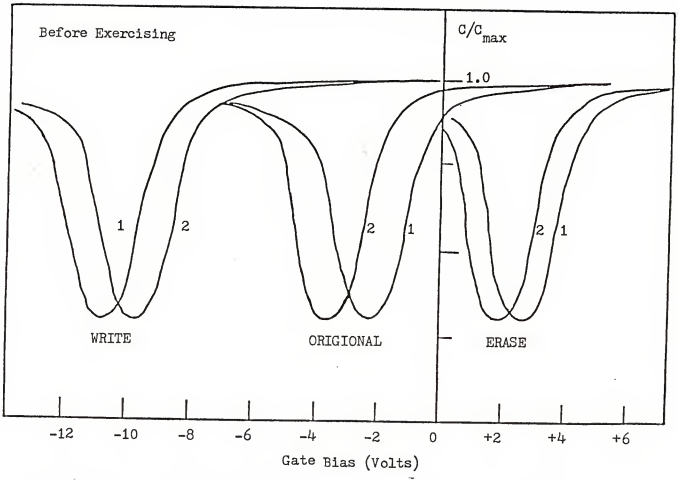


Figure 3.8 The C-V characteristics of a gridded MNOS capacitor, trace 1 was made 10 seconds after programming, trace 2 was made 4 minutes after programming

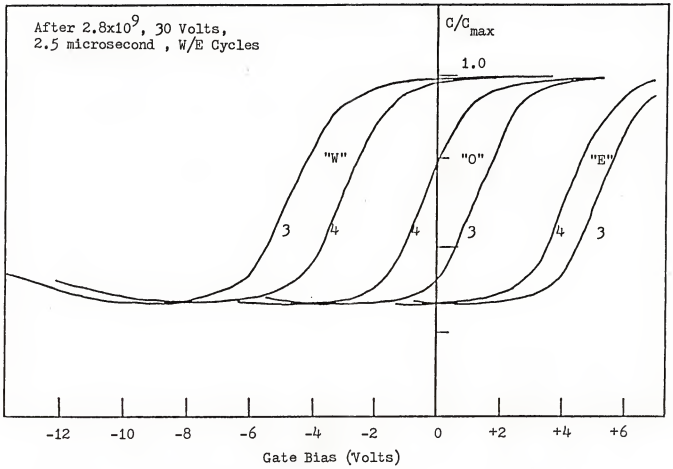


Figure 3.9 The C-V characteristics of a gridded MNOS capacitor after exercising 2.8×10^9 cycles, trace 3 was made 10 seconds after programming, trace 4 was made 4 minutes after programming

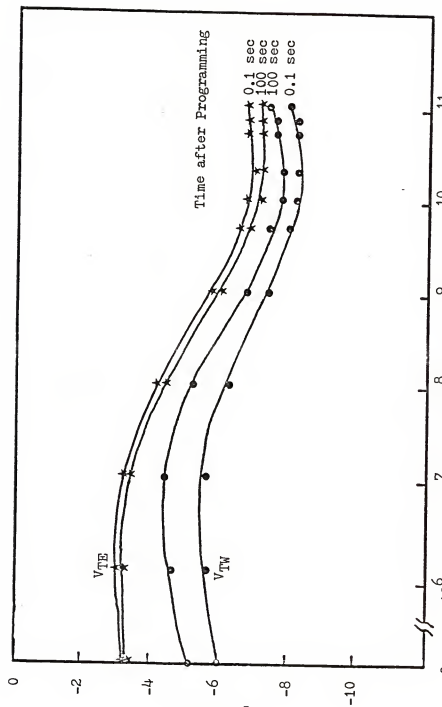


Figure 3.10 Threshold voltage vs number of W/E cycles, where the pulse amplitude is 25 volts, pulse width is 1 microsecond

in pulse width. It is observed that the upper two curves collapse to the lower two curves as a function of time after programming. For the first 10^7 endurance cycles, there was little change in the initial threshold voltage readings, but a moderate narrowing of the memory window was observed for the 100 second pulse data points. This indicates a reduction in device retention characteristics. From 10^7 up to about 10^{10} W/E cycles, initial ΔV_T is smaller, in association with a further narrowing of the 100 second memory window and a decided negative shift in the absolute threshold voltages in both the written and erased states. Beyond 10^{10} cycles, the absolute threshold voltages stabilized, or even shifted slightly in the positive direction, and the 100 second threshold voltage window continue to narrow. Eventually it collapses. The latter effect indicates further reduction of retention.

Figure 3.11 shows the window decay for four different W/E cyclings versus time after programming. The slopes indicate the decay rate, and ΔV_T is the window size. The more cycles exercised on device, the more rapidly ΔV_T drops. For 10^{10} W/E cycling, the retention ability is less than hundreds of seconds in this case.

A thorough understanding of the interface states related failure mechanisms in an MNOS device will provide us with key information for improving device performance and optimizing the fabrication process. The principles of CC-DLTS technique and the results of using this technique

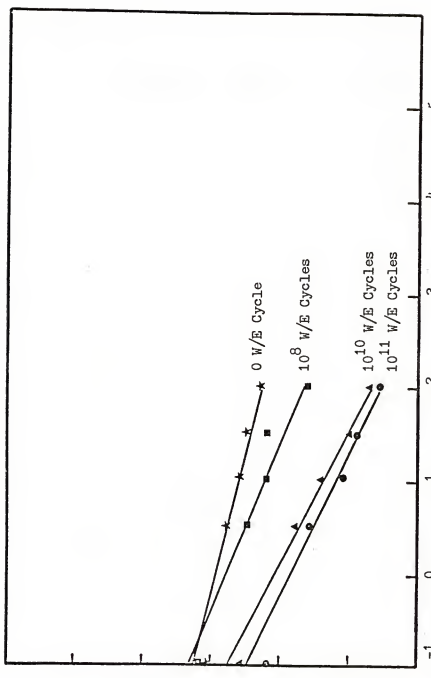


Figure 3.11 Threshold window vs time after programming, the DSP MNOS transistor was exercised under 25 volts, 1 μsec pulsing, and programmed under 25 volts, 10 μsec pulsing

for interface states analysis on the exercised MNOS capacitors will be discussed in detail in next chapter.

CHAPTER IV
THE CONSTANT-CAPACITANCE DEEP LEVEL
TRANSIENT SPECTROSCOPY TECHNIQUE

4.1 Introduction

Since the MNOS memory device is constructed with a very thick nitride insulating layer and an ultra thin ($\sim$ 20 Å) oxide layer in between the silicon substrate and nitride insulating layer, the most damage is expected to be at the silicon-oxide interface caused by the high-field operation. This may lead to a significant change of MNOS memory characteristics such as endurance, retention time, and channel conduction. Therefore, the investigation of interface states vs W/E cycling becomes the focal point of this study.

The Deep-Level Transient Spectroscopy (DLTS) and the Quasi-static Capacitance Voltage (i.e. QSCV) techniques have been employed to measure trap states at the silicon-oxide interface in the MOS capacitors [51-52]. The QSCV method has been extensively documented and has been a basic tool employed in measuring the interface state density distribution over the central portion of the semiconductor bandgap with a sensitivity of typically 1×10^{10} $ev^{-1}cm^{-1}$. As the bandedges are approached, the results become increasingly more sensitive to measurement

accuracy and uncertainties in device parameters, which render the computed distribution unreliable near the bandedges. Furthermore, the QSCV technique does not yield quantitative information on the dynamic properties of interface states. For the MNOS capacitors studied here we have found that the capacitance vs voltage curves depend strongly on the frequency for frequencies greater than 1MHz. This is due to the series resistance effect in these MNOS devices. In addition, the insulator instability is pronounced by the presence of slow states at the SiO_2 layer and becomes manifest in the hysteresis C-V curves. Having this type of instability it is difficult to distinguish between fast and slow surface states from the C-V curves.

Another observation on the measured C-V data for the MNOS capacitor is that values of capacitance determined by the QSCV method in the strong accumulation region were found to be two to three times higher than those determined by the high frequency capacitance measurements as shown in Figure 4.1. The reason for this discrepancy may be attributed to the charge exchange between memory traps and thin oxide layer or charge motion within the oxide layer such that the quasi-static capacitance value will increase as well.

The P^+-grid N-type MNOS capacitor contains different carrier transport mechanism from that of the conventional MIS structure while biasing in weak inversion and strong inversion regions. Thus, it is inadequate to use the QSCV

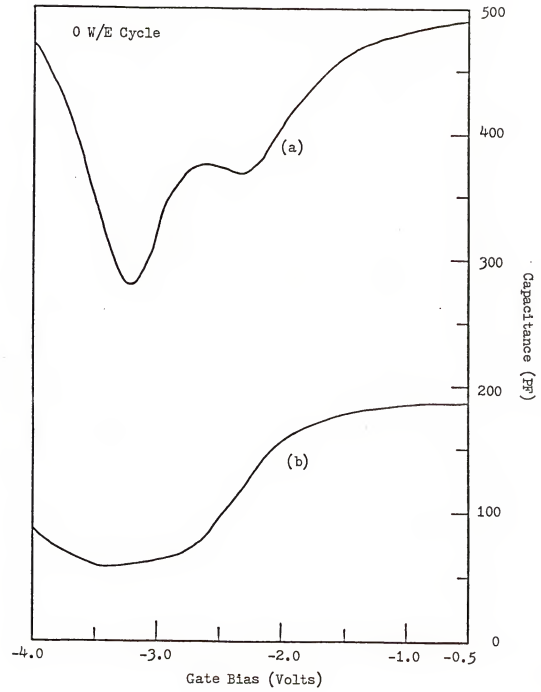


Figure 4.1 The C-V measurements on a P^{+}-base gridded MNOS capacitor (a) quasi-static C-V curve, (b) high frequency C-V curve measured at 1 MHz

method to characterize the interface states in an MNOS device. However, the QSCV technique can be used for preliminary evaluation of the MNOS devices in preparation for DLTS analysis.

The DLTS technique has only recently been applied to measure the interface states in the MOS structure [23-26], and none has been reported in the literature for the MNOS devices. For interface states studies, the DLTS measurement is performed in the constant-capacitance mode, termed CC-DLTS, which is essential for measuring continuously distributed interface traps. There is a lack of specificity of the trap level, giving rise to the DLTS emission signal. The CC-DLTS measurement yields an emission time-constant spectrum which depends on both trap distribution and capture cross section. The problem was partially analyzed by Schulz and Johnson [25] for the case of continuously distributed traps at a semiconductor-insulator interface. In their experiment on the MOS capacitor, the CC-DLTS technique has shown significant advantages over the conventional capacitance transient mode of measurement for the interface state characterization.

In this chapter, diagnostic tool for characterizing the interface states and deep-level traps in an MNOS capacitor will be described. An improved model for calculating the interface state density and the capture cross section from the CC-DLTS data will also be depicted.

4.2 Theory of the Constant-Capacitance DLTS Technique

To quantitatively examine the $Si-SiO_2$ interface states, the conventional DLTS technique has been extended to the constant-capacitance DLTS technique. We refer to the original workers, Lang [51-52] and Johnson et al.[53] and modify their theories. We derive the voltage transient in terms of the surface state densities, thermal scan temperature, DLTS signals and device parameters. Using the energy-dependent and temperature-dependent electron capture cross section, the energy-dependent interface state density in the upper half bandgap is determined from the CC-DLTS experiment.

In the conventional DLTS measurement of surface states at $Si-SiO_2$ interface, the recorded signal arises from the majority-carrier emission from traps that have emission rates located within an exponentially selected rate window. In the experiment, an MNOS capacitor is biased into depletion and periodically pulsed into strong accumulation long enough to populate all the interface traps with majority carriers. The DLTS signal is obtained by forming the difference of the gate-voltage transient measured at two delay times t_1 and t_2 after a charging pulse. The delay time defines an emission rate window given by the expression [52]

$$e_o=\ln(t_1/t_2)/(t_1-t_2) \qquad (4.1)$$

From the principle of detailed balance, the emission rate for the electrons trapped in an energy E below the semiconductor conduction bandedge is given by

$$e_n = \sigma_n \langle v_n \rangle N_c \exp(-E/kT) \qquad (4.2)$$

where σ_n is the electron capture cross section, $\langle v_n \rangle$ is the mean thermal velocity of electrons, N_c is the effective density of the conduction band states. Interface traps for which $e_n = e_o$ contribute to the DLTS signal, and the trap distribution is profiled by scanning the temperature.

In a CC-DLTS system, the depletion capacitance of the semiconductor is held constant during the transient response, the change in gate voltage required to maintain a constant capacitance appears across the double insulating layer, and the emission signal ΔV_g is related to the net charge (per unit area) in interface states, Q_{ss}, as follows:

$$\Delta V_g = (1/C_I) \times \left[Q_{ss}(t_1) - Q_{ss}(t_2) \right] \qquad (4.3)$$

where C_I is the total capacitance per unit area of two insulators, namely, the Si_3N_4 layer in series with SiO_2 layer. The gate-voltage transient is thus linearly proportional to the difference in the net charge in interface states at the two delay times t_1 and t_2 after a charging pulse. This linear dependence is obtained for all

interface trap densities, and the proportionality factor is independent of substrate doping and temperature. In contrast, in DLTS transient-capacitance measurements with fixed gate voltage, linearity is lost at high interface-state densities, and the proportionality factor depends on substrate doping density and varies with temperature.

For electron emission from a continuous distribution of interface traps, the CC-DLTS signal is

$$\Delta V_g = \frac{1}{C_I} \int_{E_v}^{E_c} qN_{ss}(E) \left[\exp\left(\frac{-t_1}{\tau_n}\right) - \exp\left(\frac{-t_2}{\tau_n}\right)\right] dE \tag{4.4}$$

where τ_n is the electron emission time constant which has the inverse relation with e_n given by Equation (4.2). Now let

$$S(E,T) = \exp(-t_1/\tau_n) - \exp(-t_2/\tau_n) \tag{4.5}$$

then Equation (4.4) can be rewritten as

$$\Delta V_g = \frac{q}{C_I} \int_{E_v}^{E_c} N_{ss}(E) S(E,T) dE \tag{4.6}$$

The S(E,T) is a sharp peak electron-emission function with respect to a specific time constant setting, t_1. If we assume that $N_{ss}(E)$ varies slowly in a small range of ΔE, and ΔE is smaller than kT, then, the approximation of Equation (4.6) is justified and becomes

$$\Delta V_g (E) = \frac{q}{C_I} [N_{ss}(E) B\ kT] \tag{4.7}$$

where

$$B \triangleq \frac{\int_{E_v}^{E_c} S(E,T)\,de}{kT} \tag{4.7a}$$

Therefore, the interface state density at energy level E in the bandgap, $N_{ss}(E)$, is obtained in terms of $\Delta V_g(E)$, B, elctronic charge q, Boltzmann constant, k, and temperature, T. For a given temperature, the surface state density can be profiled across the Si bandgap by combining Equations (4.1), (4.2), (4.7) and (4.7a) provided that the capture cross section is known. It has been shown that the capture cross section in general depends on energy as well as temperature, and can be expressed as

$$\sigma_n(E,T) = \sigma_o (E) \exp(\frac{-\Delta E_\sigma}{kT}) \tag{4.8}$$

Detailed discussions are given in the next section. It is assumed that $N_{ss}(E)$ varied slowly over an energy interval less than the order of kT and only those interface states located within this energy interval ΔE contribute to the emission signal.

The energy resolution is therefore greatest at low temperatures where the sample interval is the closest to

the conduction band and the interface state density is expected to vary most rapidly. The larger energy interval obtained at high temperature provides enhanced sensitivity for detecting low densities of interface states which are found near midgap.

4.3 Determination of Capture Cross Section for Surface State Energy Distribution

Determination of trap parameters for surface states which are continuously distributed in energy encounters some difficulties since the DLTS spectrum consists of many contributions from many states with different capture cross sections and different activation energies. To overcome these difficulties, the energy resolved DLTS technique has been proposed [23]. However, the capture cross section is not able to determine independently and uniquely by this technique. Schulz and Johnson [25] reported that the capture cross section depends on temperature rather than on energy, which is contradictory to Wang's results [23]. Wang reported that the capture cross section depended on energy but not on temperature. Energy-dependent capture cross section was also measured by the conventional conductance method [16], where no temperature dependence was considered.

In our experiment, the interface state densities were obtained in terms of different emission rate selection. In the translation of temperature scans into energy

distribution, we found that neither the temperature dependence nor the energy dependence is applicable. Therefore, we believe that the electron capture cross section isboth energy-dependent and temperature-dependent.

Measurements of electron capture cross sections at surface states in MOS diodes were reported recently using the small amplitude injection-pulse DLTS technique [54]. The technique enables one to determine energy and temperature dependence of capture cross section separately. Applying this method to the MNOS memory capacitor, the temperature-dependent and energy-dependent capture cross section at the Si-SiO_2 interface was obtained and confirmed.

4.3.1 Theoretical background

An MNOS capacitor is biased for constant surface potential under the depletion condition, and small voltage pulses (injection pulses) ΔV are applied in such a way that surface states in a narrow energy range ΔF_F are filled with majority carriers (electrons in the present case) as illustrated in Figure 4.2(a), and the capacitance transient is shown in Figure 4.2(b). The capacitance difference between two gating times, t_1 and t_2, contributed to the DLTS signal is given by[52]

$$\Delta C = A \int_{E_v}^{E_c} N_{ss}(E) \left[\exp\left(\frac{-t_1}{\tau_n}\right) - \exp\left(\frac{-t_2}{\tau_n}\right)\right] x[f_o(E) - f_1(E)]dE \qquad (4.9)$$

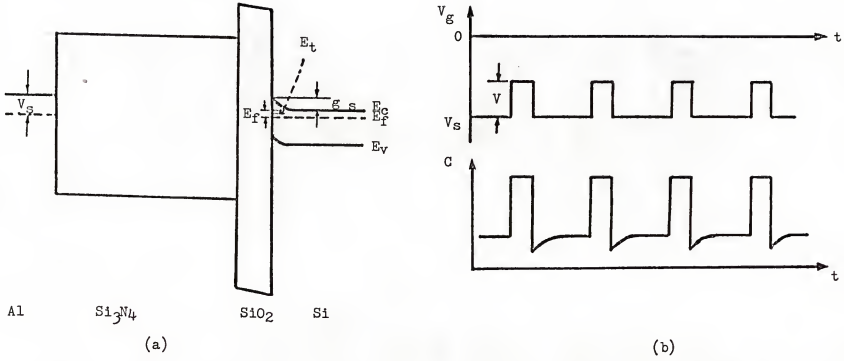


Figure 4.2 The small amplitude injection-pulse DLTS for determining capture cross section of the trap states at the Si-SiO_2 interface of an MNOS capacitor (a) energy band diagram under small pulse biasing, (b) gate bias and capacitance transient during the DLTS measurement

where $N_{ss}(E)$ is the surface state density at energy E, τ_n is the emission time constant of electrons, E_c and E_v are conduction and valence band edges, respectively; E_F is the Fermi level, and f_o and f_1 are the electron occupation functions at surface states when the surface potential is given by ϕ_s and $\phi_s - \Delta E_f/q$, respectively,

$$f_o(E) = [1 + \exp(\frac{E-E_F}{kT})]^{-1} \tag{4.10}$$

$$f_1(E) = [1 + \exp(\frac{E-E_F + \Delta E_F}{kT})]^{-1} \tag{4.11}$$

When the injection pulse height is small enough, $f_o(E)-f_1(E)$ can be assumed as a function of $(E-E_t)$, where $E_t=E_F+1/2\,\Delta E_F$, and Equation (4.1) reduces to

$$\Delta C = AN_{ss}(E)[\exp(-\frac{t_1}{\tau_n} - \exp(-\frac{t_2}{\tau_n})] \tag{4.12}$$

which is the same expression as for a discrete level [52]. Thus the conventional analysis is applied, and the DLTS spectrum has a peak [52] at

$$\tau_n = \frac{t_2 - t_1}{\ell n\,(T_2/t_1)}$$

The emission time constant τ_n can be expressed by

$$\tau_n = [\sigma_n \langle v_n \rangle N_c \exp(-\frac{\Delta E_t}{kT})]^{-1} \quad (4.13)$$

where ΔE_t is the activation energy which is defined by

$$\begin{aligned} \Delta E_t &= E_c - E_t \\ &= q\phi_s + (E_c - E_F) - 1/2\Delta E_F \end{aligned} \quad (4.14)$$

The capture cross section is assumed to be energy dependent in the pre-exponential term and temperature dependent exponentially as Equation (4.8); thus ,it can be written as

$$\sigma_n (E_t,T) = \sigma_o(E_t) \exp(\frac{-\Delta E_\sigma}{kT}) \quad (4.15)$$

where ΔE_σ is a constant which stands for the thermal activation energy of capture cross section. It is further assumed that shallow impurities are dominant in the bulk and are all ionized, the effective density of states in conduction band, N_c (cm^{-3}), can be approximated as

$$N_c \simeq N_D \exp[\frac{(E_c-E_F)}{kT}] \quad (4.16)$$

Substituting Equations (4.13) - (4.15) into Equation (4.12) yields

$$\begin{aligned} \tau_n = \{&\langle v_n \rangle N_D \sigma_o(E_t) \\ &\times \exp[-(\Delta E_\sigma + q\phi_s - \frac{1}{2}\Delta E_F)/kT]\}^{-1} \end{aligned} \quad (4.17)$$

Thus, the slope of the Arrhenius plot, $\ln(e_n/T^2)$ vs T^{-1}, gives an apparent activation energy $\Delta E_\sigma + q\phi_s - 1/2\Delta E_F$ and the intersection with the $\ln(e_n/T^2)$ axis provides $\rho_o(E_t)$ can be obtained as a function of E_t when the measurement is carried out by varying the bias voltage. To deduce ΔE_σ, the surface potential ϕ_s should be measured from the capacitance-voltage characteristics at temperatures where the DLTS spectrum exhibits a peak. An empirical equation is deduced for $\sigma_o(E_t)$ as [54]

$$\sigma_o(E_t) = 2.6\times10^{-18} \exp[10.5(E_c - E_t)] \qquad (4.18)$$

where $E_c - E_t$ is in eV. It shows that the energy-dependent cross section $\sigma_o(E_t)$ decreases exponentially towards the conduction band edge, and the energy-dependent term has been separated from the temperature-dependent term in the capture cross section.

4.3.2 Determination of ΔE_σ

The parameter ΔE_σ in the exponential term of capture cross section plays an important role in locating the energy distribution in the Si band gap. Schulz and Johnson [25] assumed $\Delta E_\sigma = 89$ meV. A positive value of ΔE_σ is interpreted by a multiphonon emission model. The MOS devices they used for experiment are the simple capacitor structure. Katsube et al. [54] suggested capture cross sections can be projected to room temperature or any other

temperature. They used a negative value of ΔE_σ to determine the capture cross section and attributed it to cascade phonon capture. We modify their results empirically.

The thermal scans of voltage transient from 77°K up to 400°K were carried out with three different rates window. The data are shown in Figure 4.3, where rate windows t_1/t_2 were set to be 5ms/10ms, 10ms/20ms, and 25ms/50ms. The MNOS capacitors under investigation were fabricated with P^+-grid diffusion in N type substrate. The grids contact was tied electrically to the substrate. When an inversion gate bias was applied, the minority carriers (holes) can be supplied from P^+-grid to the inversion surface even at 20MHz frequency range.

Whenever the emission signal is contributed from those electrons in traps near midgap, holes supplied from P^+-grids will recombine with captured electrons . The number of carriers involves in recombination process depends upon how strong the inversion is reached. Thus, very few electrons will emit to the conduction band. The voltage transient signal is reduced and approaches zero when the scanning temperature is higher than room temperature. This phenomenon is illustrated in Figure 4.3. For time constants, t_1=10ms and t_2=20ms, Figure 4.3 shows the electron emission from the midgap traps at room temperature; as minority carriers (i.e., holes) begin to recombine with the majority carriers (i.e., electrons)

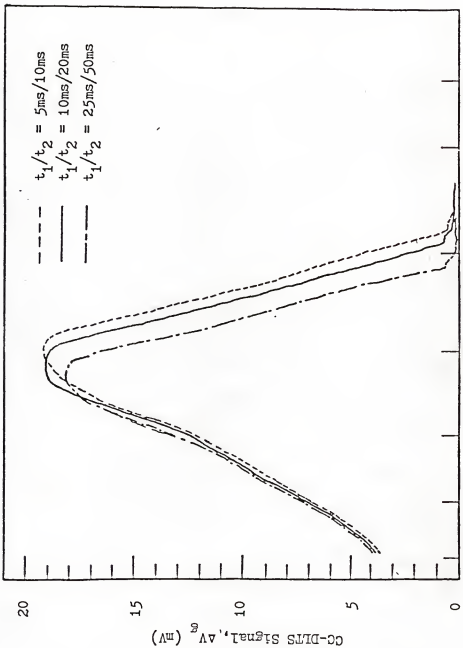


Figure 4.3 The CC-DLTS spectra of thermal scan obtained from a nonexercised P^+-base gridded MNOS capacitor with three different rate windows

captured in the traps at the effective recombination center (near the midgap), the onset recombination behavior results in a drastic decrease of the CC-DLTS signal. In this figure, ΔV_g is shown to be very small and approaches zero.

In the previous section, E is defined as the trap energy level below the conduction-band minimum, and $\Delta E_t = E_c - E_t$. For any peak signal in the CC-DLTS spectrum [53]

$$\Delta E_t = kT\ell n(\sigma_n < V_n > N_c \, t_1/\ell n2) \tag{4.19}$$

where the rate window is set at $t_2 = 2t_1$.

Substituting Equations (4.15) and (4.18) into (4.19) yields

$$\Delta E_t = \frac{1}{(1 - 10.5\ kT)} \left[kT\ell n(<V_n>N_c t_1/\ell n2) - \Delta E_\sigma - 40.5kT\right] \tag{4.20}$$

According to Figure 4.3 and Equation (4.20), for $\Delta E_t = 0.56$ev at T=300K, ΔE_σ is calculated with a positive value of 0.036ev.

4.4 Determinationof Surface State Density

In section 4.1, we analyze the relationship between the CC-DLTS signal $\Delta V_g(E)$ and the surface state density $N_{ss}(E)$ by defining B(T) in Equation (4.7a). Rewrite the DLTS signal S(E,T) with respect to energy and temperature;

$$S(E,T) = \exp\left[\frac{-t_1}{\tau_n(E)}\right] - \exp\left[\frac{-t_2}{\tau_n(E)}\right] \tag{4.21}$$

where $\tau_n = [\sigma_n < V_n > N_c \exp(\frac{-E}{kT})]^{-1}$ (4.22)

$$\sigma_n = \sigma_o(E) \exp(-\frac{\Delta E_\sigma}{kT}) \quad (4.23)$$

$$\sigma_o(E) = 2.6 \times 10^{-18} \exp(10.5E) \quad (4.24)$$

$$\Delta E_\sigma = 0.036 \text{ eV} \quad (4.25)$$

$$t_2 = 2t_1 \quad (4.26)$$

$$<V_n> = \frac{\sqrt{3kT}}{M_c^*} = 1.324 \times 10^6 T^{1/2} \quad (4.27)$$

$$N_c = 2(\frac{2\pi M_{de}^* kT}{h^2})^{3/2} = 5.39 \times 10^{15} T^{3/2} \quad (4.28)$$

Substituting these parameters into S(E,T), we have

$$S(E,T) = \exp(-1.85 \times 10^4 T^2 t_1 Y) - \exp(-3.7 \times 10^4 T^2 t_1 Y) \quad (4.29)$$

where $Y = \exp[10.5E - (E + 0.036)/kT]$.

The spectrum S(E,T) is contributed fromthe electron emission in a narrow energy range which has a sharp peak at a specific temperature in the DLTS scan. For example, if time constant t_1=10msec and t_2=20msec, the thermal emission of electrons at energy E has maximum emission temperature which is illustrated in Figure 4.4 for six different energy

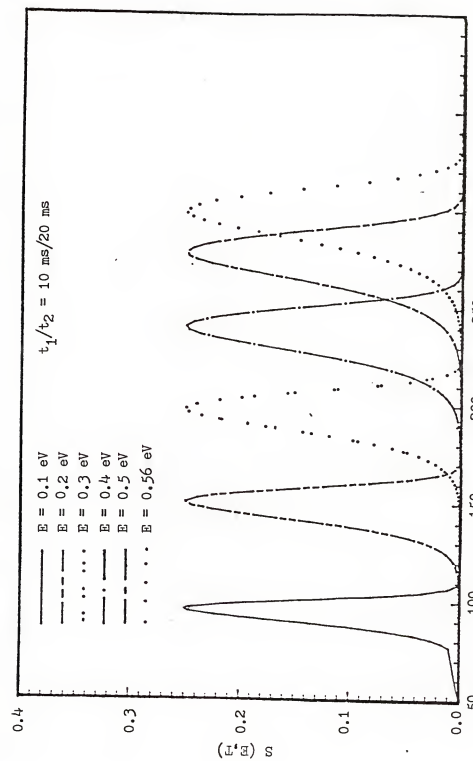


Figure 4.4 The emission spectra from six different trap levels presenting in the thermal scan of CC-DLTS measurements, rate window $t_2 = 2t_1 = 20$ ms

levels. Figure 4.5 provides another view of the spectra S(E,T) in which it clearly shows that the area under each emission curve exactly presents the amount of emission at a particular temperature. In addition, only a small range of energy levels effectively dominates the thermal emission.

The CC-DLTS spectra calculated from Equation (4.29) is shown in Figure 4.5. A linear relation of B and T was obtained using Equation (4.7a) and Equation (4.29), and was plotted in Figure 4.6, which is deduced as

$$B(T) = 0.65 + T \times 10^{-3} \tag{4.30}$$

Finally, the surface state density $N_{ss}(E)$ is defined as

$$N_{ss}(E) = \left(\frac{C_I}{qk}\right) \frac{\Delta V_g(T)}{TB(T)} \tag{4.31}$$

The energy profile for $N_{ss}(E)$ from the CC-DLTS spectra can be written as

$$\Delta E_t = \left(\frac{1}{1-10.5kT}\right)\{kT[\ln(\langle V_n \rangle N_c t_1/\ln 2) - 40.5] - 0.036\} \tag{4.32}$$

The relation between temperature T and trap energy $\Delta E_t(T,t_1)$ is listed in Table 4.1 with respect to each selected time constant setting t_1 in the DLTS measurement. Using this table, the CC-DLTS signals can be scaled on

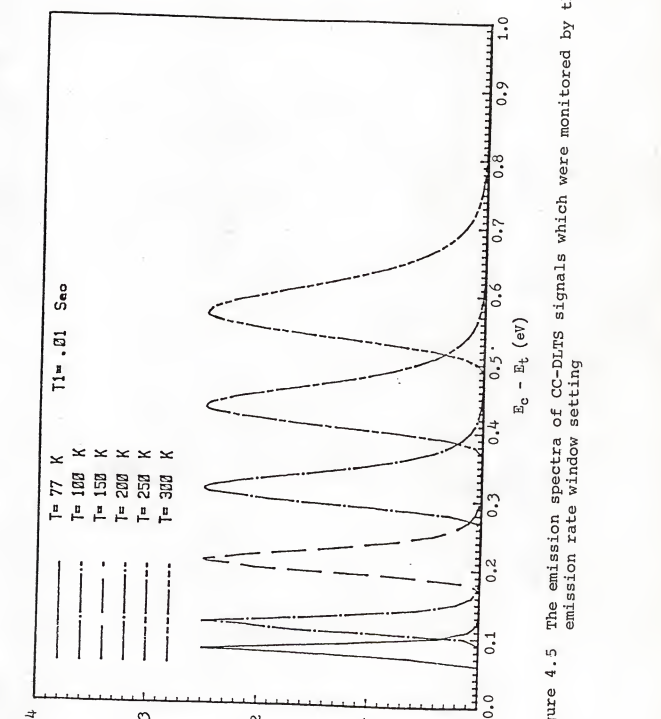


Figure 4.5 The emission spectra of CC-DLTS signals which were monitored by the emission rate window setting

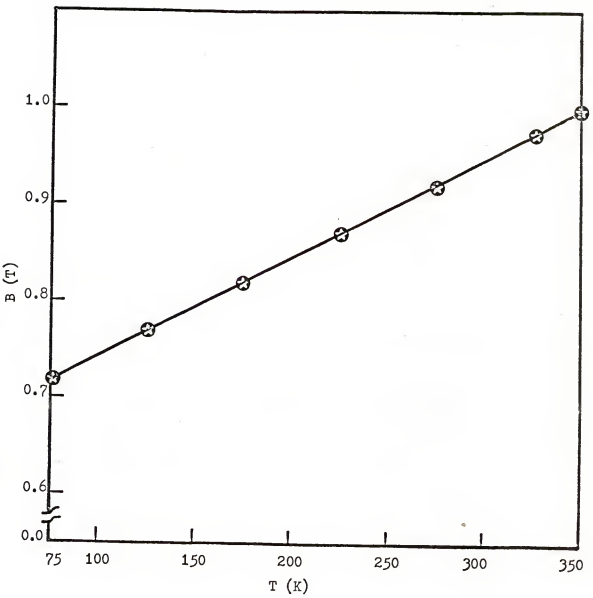


Figure 4.6 The relationship between B(T) and temperature

TABLE 4.1

Surface State Energy Distribution E_t vs Temperature and Rate Window

Temp.(^{o}K)	t_1=1ms	t_1=2.5ms	t_1=5ms	t_1=10ms	t_1=25ms
77.5	.047	.054	.059	.064	.070
80.0	.051	.058	.063	.068	.075
82.5	.054	.061	.066	.072	.079
85.0	.058	.065	.070	.076	.083
87.5	.061	.069	.074	.080	.087
90.0	.065	.072	.078	.084	.092
92.5	.068	.076	.082	.088	.096
95.0	.072	.080	.086	.092	.100
97.5	.075	.084	.090	.096	.105
100.0	.079	.087	.094	.101	.109
102.5	.082	.091	.098	.105	.114
105.0	.086	.095	.102	.109	.118
107.5	.090	.099	.106	.113	.123
110.0	.094	.103	.110	.118	.127
112.5	.097	.107	.115	.122	.132
115.0	.101	.111	.119	.127	.137
117.5	.105	.115	.123	.131	.141
120.0	.109	.119	.127	.135	.146
122.5	.113	.124	.132	.140	.151
125.0	.117	.128	.136	.145	.156
127.5	.121	.132	.140	.149	.160
130.0	.124	.136	.145	.154	.165
132.5	.128	.140	.149	.158	.170
135.0	.133	.145	.154	.163	.175
137.5	.137	.149	.158	.168	.180
140.0	.141	.153	.163	.172	.185
142.5	.145	.158	.167	.177	.190
145.0	.149	.162	.172	.182	.195
147.5	.153	.167	.177	.187	.200
150.0	.157	.171	.181	.192	.205
152.5	.162	.176	.186	.197	.211
155.0	.166	.180	.191	.202	.216
157.5	.170	.185	.196	.207	.221
160.0	.174	.189	.200	.212	.226
162.5	.179	.194	.205	.217	.232
165.0	.183	.199	.210	.222	.237
167.5	.188	.203	.215	.227	.242
170.0	.192	.208	.220	.232	.248
172.5	.197	.213	.225	.237	.253
175.0	.201	.218	.230	.242	.259
177.5	.206	.222	.235	.248	.264
180.0	.210	.227	.240	.253	.270
182.5	.215	.232	.245	.258	.276
185.0	.220	.237	.250	.264	.281

TABLE 4.1 (Continued)

187.5	.224	.242	.256	.269	.287
190.0	.229	.247	.261	.274	.293
192.5	.234	.252	.266	.280	.298
195.0	.238	.257	.271	.285	.304
197.5	.243	.262	.277	.291	.310
200.0	.248	.267	.282	.297	.316
202.5	.253	.273	.287	.302	.322
205.0	.258	.278	.293	.308	.328
207.5	.263	.283	.298	.314	.334
210.0	.268	.288	.304	.319	.340
212.5	.273	.294	.309	.325	.346
215.0	.278	.299	.315	.331	.352
217.5	.283	.304	.321	.337	.358
222.5	.293	.315	.332	.349	.371
225.0	.298	.321	.338	.355	.377
227.5	.304	.326	.343	.361	.383
230.0	.309	.332	.349	.367	.390
232.5	.314	.337	.355	.373	.396
235.0	.320	.343	.361	.379	.402
237.5	.325	.349	.367	.385	.409
240.0	.330	.355	.373	.391	.415
242.5	.336	.360	.379	.397	.422
245.0	.341	.366	.385	.404	.429
247.5	.347	.372	.391	.410	.435
250.0	.352	.378	.397	.416	.442
252.5	.358	.384	.403	.423	.449
255.0	.364	.390	.410	.429	.456
257.5	.369	.396	.416	.436	.462
260.0	.375	.402	.422	.442	.469
262.5	.381	.408	.428	.449	.476
265.0	.387	.414	.435	.456	.483
267.5	.392	.420	.441	.462	.490
270.0	.398	.426	.448	.469	.497
272.5	.404	.433	.454	.476	.504
275.0	.410	.439	.461	.483	.512
277.5	.416	.445	.467	.490	.519
280.0	.422	.452	.474	.497	.526
282.5	.428	.458	.481	.504	.533
285.0	.434	.465	.488	.511	.541
287.5	.440	.471	.494	.518	.548
290.0	.447	.478	.501	.525	.556
292.5	.453	.484	.508	.532	.563
295.0	.459	.491	.515	.539	.571
297.5	.466	.498	.522	.546	.578
300.0	.472	.504	.529	.554	.586
302.5	.478	.511	.536	.561	.594
305.0	.485	.518	.543	.568	.602
307.5	.491	.525	.550	.576	.610
310.0	.498	.532	.558	.583	.617
312.5	.504	.539	.565	.591	.625
315.0	.511	.546	.572	.599	.633

TABLE 4.1 (Continued)

317.5	.518	.553	.580	.606	.641
320.0	.525	.560	.587	.614	.650
322.5	.531	.567	.595	.622	.658
325.0	.538	.575	.602	.630	.666
327.5	.545	.582	.610	.638	.674
330.0	.552	.589	.617	.645	.683
332.5	.559	.597	.625	.653	.691
335.0	.566	.604	.633	.662	.700
337.5	.573	.612	.641	.670	.708
340.0	.580	.619	.648	.678	.717
342.5	.588	.627	.656	.686	.725
345.0	.595	.634	.664	.694	.734
347.5	.602	.642	.672	.703	.743
350.0	.609	.650	.681	.711	.752

energy below the conduction band minimum from 75K up to 350K. Figure 4.7 is the plot of the measured surface state densities $N_{ss}(E)$ vs temperature with three different Boxcar averager time constant settings on an unexercised P^+-emitter gridded MNOS capacitor. Figure 4.8 illustrates the excellent data fitting with ΔE_σ =0.036eV after the temperature scale is converted into energy distribution in the upper half band gap of silicon. In this case, we observed a peak density at 0.37eV below the conduction-band minimum. The surface state densities for this MNOS device are in the range of $2.0x10^{10}$ to $1x10^{12}$ $cm^{-2}eV^{-1}$ which is an order of magnitude higher than that of the conventional MOS device.

The capture cross section measured by the CC-DLTS technique is under high electric field condition (in the order of 10^5 V/cm). Therefore, there might be a distortion of capture cross section due to the applying gate bias. The value obtained for the capture cross sections at $Si-SiO_2$ interface is in the range of $3x10^{-16}$ cm^2 to $3x10^{-18}$ cm^2, as is shown in Figure 4.9. The majorities of traps in this range are neutral-type. Their capture radius is of the order of atomic dimension (10^{-8} cm). The capture cross sections should exhibit weaker electric field dependence than Coulombic attractive centers since the capture radius should be a weaker function of electric field strength [55]. This result rules out the possibility of an inaccurate capture cross section measurement owing to high stress by the CC-DLTS method.

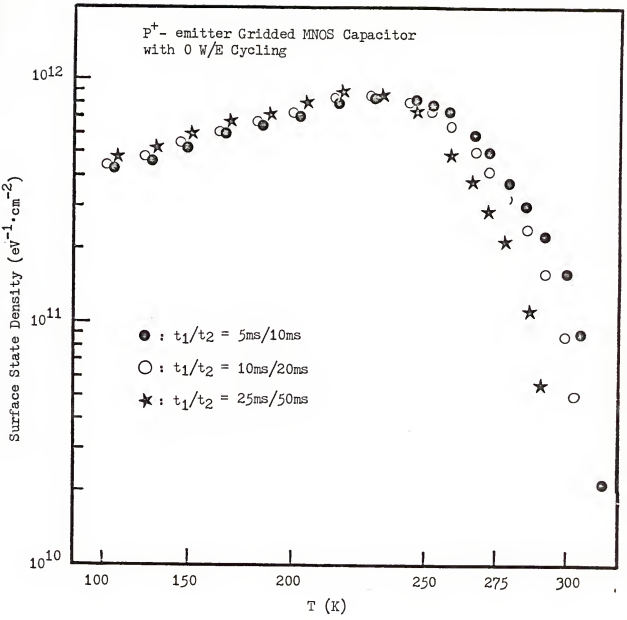


Figure 4.7 The surface state densities vs temperature curves as deduced from the CC-DLTS measurements on non-exercised P^+-base gridded MNOS capacitor

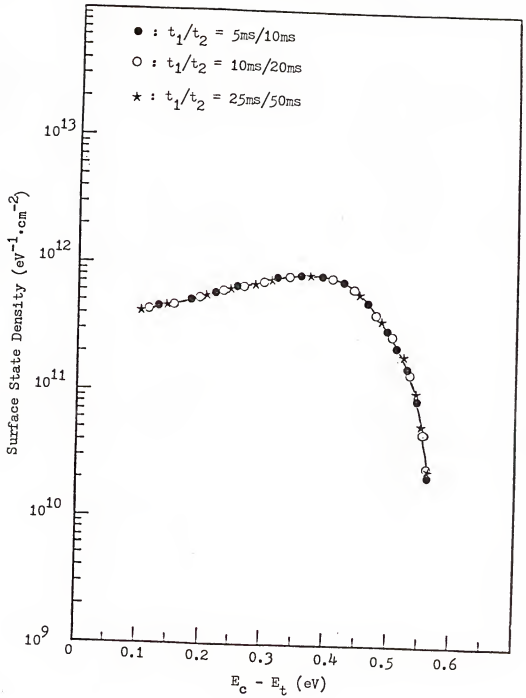


Figure 4.8 The converted surface state densities vs energy below the conduction band minimum of silicon with ΔE_σ = 0.036 eV

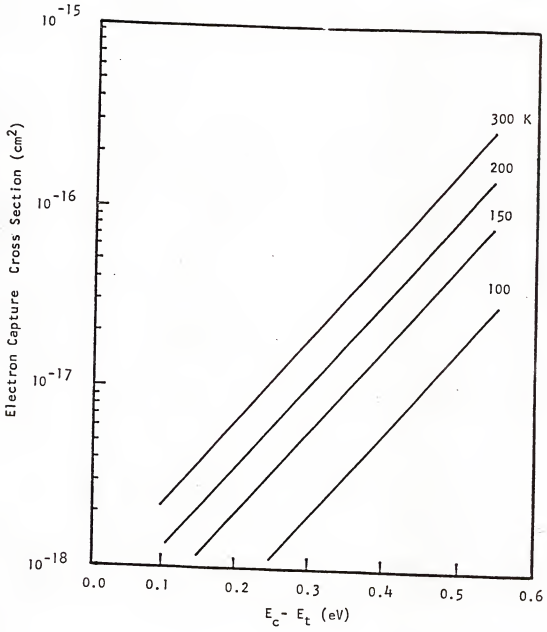


Figure 4.9 The electron capture cross sections of surface state traps in upper half bandgap on an MNOS capacitor plotted as functions of energy and temperature

Figure 4.10 shows two CC-DLTS thermal scans on a P^+-emitter gridded MNOS capacitor with two different rate windows, t_1/t_2=2.5 ms/5.0 ms and t_1/t_2=10 ms/20 ms. This capacitor has been exercised by $5x10^8$ cycles using 28 Volts, 1 sec pulse. The measured spectra in shape are similar to those shown in Figure 4.3, but the amplitudes are much larger. Figure 4.11 shows the other two thermal scans on a P^+-base gridded MNOS capacitor which were also exercised under the same conditions as the one shown in Figure 4.10. Larger CC-DLTS signals are observed for the device with base diffsion than with emitter diffusion. These data in Figure 4.10 and Figure 4.11 are converted into surface state density vs energy curves and are illustrated in Figure 4.12. It is observed that the MNOS capacitor with P^+-base grids created higher surface state density near midgap than that with P^+-emitter after high voltage W/E operation. The excellent fits of data presented in Figure 4.12 proves that the energy-dependent and temperature-dependent capture cross sections can be used for calculating surface state densities in exercised MNOS devices.

A theoretical model which can be used to explain the temperature dependence of the capture cross section for the positive ΔE_σ is the lattice relaxation multiphonon emission process which has been proposed to explain the emission of electrons from the interface states in MOS structure [25]. This model assumes a neutral center

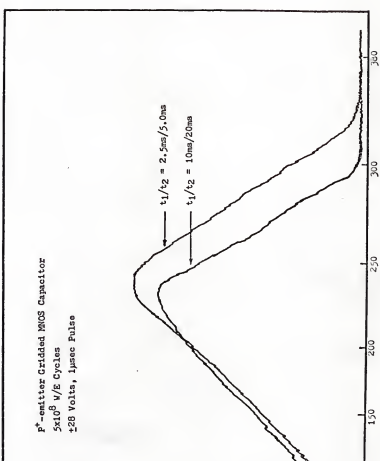


Figure 4.10 Two CC-DLTS thermal scans on exercised P^+-emitter gridded MNOS capacitor

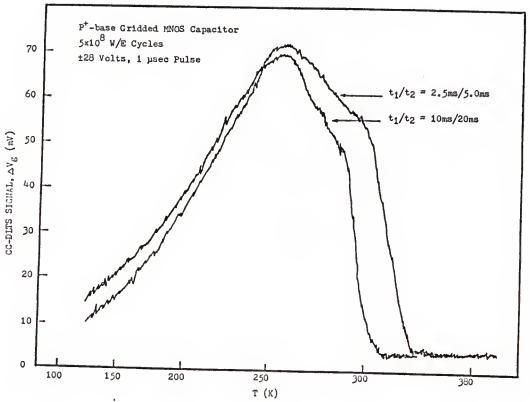


Figure 4.11 Two CC-DLTS thermal scans on exercised P^+-base gridded MNOS capacitor

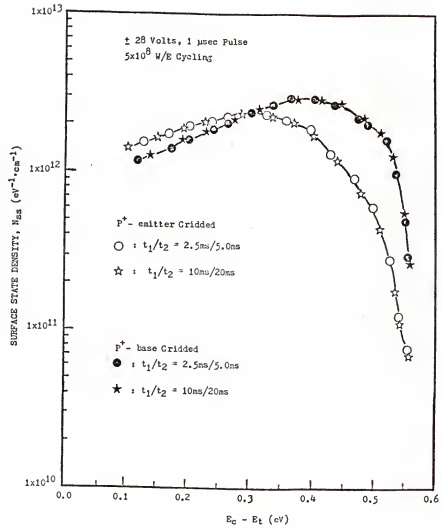


Figure 4.12 The curve fittings of surface state densities for exercised MNOS capacitors with two different diffusion processes

(acceptor type trap near the conduction band) in which the vibration of a lattice phonon modulates linearly the depth of the potential well binding the carrier. For sufficiently large vibrations which are more probable at high temperatures, the level can cross into the conduction band and capture an electron. Immediately after capture, the lattice equilibrium position changes leaving the captured carrier in a highly excited vibrational state which rapidly decays by multiphonon emission into the equilibrium state. This model is in general agreement with our experimental observation. Therefore, we conclude that the surface states in the upper half forbidden bandgap are acceptor type. This implies that those states above the Fermi level E_F are neutral while those below E_F are negatively charged.

It is noted noted that the reverse bias voltage applying to the gate during the CC-DLTS thermal scans should be sufficiently small to avoid the memory charges trapped in the SiO_2-Si_3N_4 interface tunneling back to Si substrate and vice versa. The high frequency capacitance vs voltage curves have also been taken before and after the CC-DLTS measurement to see if there is any capacitance shift. Thus, the surface state densities data should be taken with caution so that no memory states were changed. Based on the frequency independent property of the CC-DLTS measurement which will be illustrated in Chapter V, we believe that the CC-DLTS spectra are contributed from Si surface states.

CHAPTER V
RESULTS AND DISCUSSIONS OF THE CONSTANT-CAPACITANCE DEEP LEVEL TRANSIENT SPECTRSOPY(CC-DLTS) AND EXPERIMENT

5.1 Introduction

The Constant-Capacitance Deep Level Transient Spectroscopy (CC-DLTS) technique is an extension of the conventional DLTS technique which was developed by Lang [51-52] in 1974. The DLTS technique is a powerful tool for investigating deep-level traps in a p-n junction device structure. In a MIS structure, the surface states are continuously distributed in energy, and thus it is extremely difficult to employ the conventional DLTS technique to measure the surface state density and capture cross section. Therefore, a voltage transient (or constant capacitance DLTS) technique was developed by Johnson et al [53] to overcome the drawbacks of DLTS technique.

Although, the conductance and capacitance methods have been widely employed to study the MIS interface states, the CC-DLTS technique is a much more powerful tool for measuring the dynamic interface properties since it is not affected by the surface potential fluctuation. The fluctuation arises from the random spatial distribution of the fixed positive charge in the oxide.

In this chapter,a detailed description of the CC-DLTS

technique and its application for diagnosing the failure mechanisms in the exercised MNOS memory devices will be discussed. In section 5.2, the CC-DLTS apparatus is described. Section 5.3 provides experimental data on simple MNOS capacitors and P^+-gridded MNOS capacitors. The relation between surface states densities with respect to the amplitude of exercising pulse and the number of write/erase cycles are examined in section 5.4. Discussion of the results will be given in section 5.5.

5.2 The CC-DLTS Apparatus

The main feature of the DLTS experiment is the ability to set an emission rate window such that the measurement apparatus only responds when it sees a transient with a emission rate within this window. Thus, if the emission rate of a trap is varied by varying the sample temperature, the instrument will show a response peak at the temperature where the trap emission rate is within this window.

A block diagram of the apparatus is shown in Figure 5.1. The measurement system consists of a capacitance bridge with fast transient response, a pulse generator for rapidly changing the sample bias, a Boxcar averager which contains a dual gated signal integrator, an X-Y recorder, a variable temperature cryostat, a RF signal generator, two amplifiers and a feedback circuit which maintains the capacitance of an MNOS capacitor at a constant value by varying the gate voltage. It offers distinct advantages

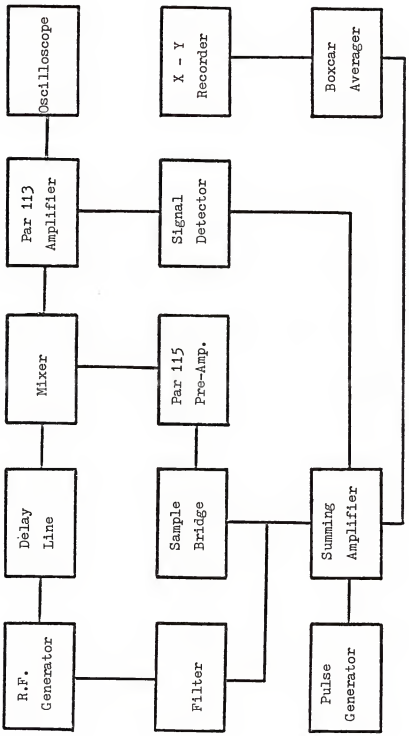
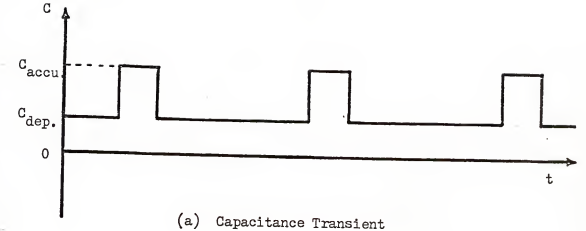


Figure 5.1 The block diagram of the CC-DLTS apparatus

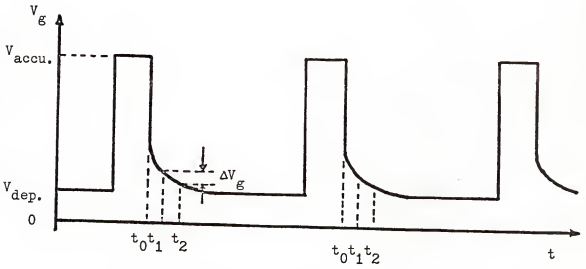
for data analysis as was illustrated in Chapter IV.

The CC-DLTS circuit consists of a conventional DLTS system [56] and a feed-back circuit which provides detection and amplification of the transient signal. The circuit functions are described as follows: Signals from the RF generator and pulse generator are added (or modulated) and introduced to the center-tap of a capacitance bridge circuit. The two arms of the nulled capacitance bridge circuit are one arm with sample in the temperature chamber and the other arm with the balancing decade and variable capacitors. The capacitance transient signal from the sample due to emission of majority carrier traps unbalances the bridge and causes a current flow that is detected by the CT-1 current transformer. The output of the CT-1 pulse transformer is superimposed on the R.F. carrier signal. This modulated signal is then amplified by a wide-band amplifier (10X or 100X). A second signal path through a 50 nsec delay line and attenuator provides the reference signal needed by the double balanced mixer to demodulate the output signal from the wide-band amplifier. The second amplifier, PAR model 113, then provides additional gain. The output signal is then monitored by the oscilloscope and is applied to the high speed, wide band feed-back circuit. The feed-back circuit is built mainly by HA-5190 operational amplifiers. The HA-5190 is a monolithic operational amplifier featuring an ultimate combination of speed, precision, and bandwidth. Employing

monolithic bipolar construction coupled with dielectric isolation, these devices are capable of delivering an unparalleled 200 V/us slow rate with a setting time of 70 nsec (0.1%, 5V output step). Other features of HA-5190 are 150 MHz gain-bandwidth-product and excellent input characteristics such as 5 mV offset voltage and 15 nV input voltage noise (at 1KHz). Therefore, the circuit can follow the signal at least up to one tenth of a microsecond. First, the transient signal due to emission is discriminated by the signal detector and amplifier, and the amplified transient signal is then superimposed on the pulse bias to compensate the capacitance transient arised from emission of majority carrier traps. Thus, the output waveform of the second amplifier will become constant during pulse biasing as shown in Figure 5.2a. The voltage transient at the output of the summing amplifier is branched and illustrated in Figure 5.2b. The branched voltage transient signal is then connected to the input of the Boxcar averager, and the output signal (i.e., the CC-DLTS signal) from the Boxcar averager is connected to the X-Y recorder. Figure 5.3a is a photograph taken at the output of PAR 113, which gives a clear picture of the correlation between the waveform of pulse bias and the capacitance transient signal. This picture shows the exponential emission of majority carrier trap right after the reverse biasing pulse. Figure 5.3b illustrates the CC-DLTS signal and the DLTS signal before feed back



(a) Capacitance Transient



(b) Voltage Transient

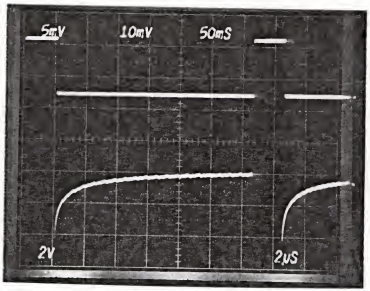
Figure 5.2 The constant capacitance transient signal and voltage transient signal in the CC-DLTS system

compensation. Figure 5.3c is the other photograph which presents the CC-DLTS voltage transient signal and the corresponding DLTS constant capacitance signal during voltage compensation.

The model 162 Boxcar averager containing two Model 164 gated integrator channels provides averaging function. During the sampling interval (integrator gated on), the channel will either exponentially or linearly charge towards the instantaneous value of the waveform. Since the transient voltage is assumed to be an exponential signal, the exponential averaging mode is always used.

The mainframe of Model 162 Boxcar controls the aperture delay for each integrator channel and its relative separation by a range switch. This establishes the rate window. The aperture delay settings are the t_1 and t_2 time. They operated as a percent of the value of time indicated by the range switch. This delay occurs after a signal is received from the triggering mode. The aperture durations and the scan time control most of the signal averaging. The aperture duration time is the length of time that each integrator is gated on. During these "on" times, the integrator tries to charge towards the instantaneous value of the input waveform. The scan time is the total time interval during which the input signal will be averaged before the integrator channels are cleared and the sequence repeats for another sampled value. These sampled values are then smoothed out by the time constant

(a)



(b)

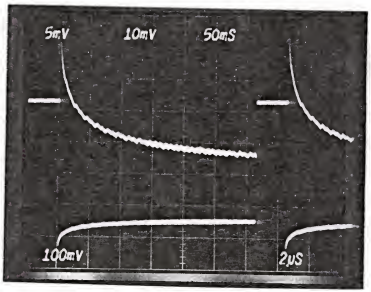


Figure 5.3 The photographs of the CC-DLTS signals (a) gate bias pulsing with 0 volt 50 ms accumulation pulse and -3 volts, 320 ms inversion pulse. Typical DLTS trap emission signal shown in the lower half screen; (b) the uncompensated DLTS signal (lower case) and feedback signal (upper case); (c) constant capacitance transient signal (upper case) and the correlated voltage transient signal (lower case)

(c)

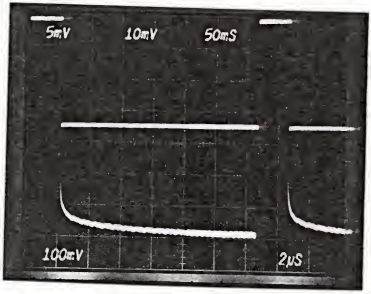


Figure 5.3—Continued

setting of the signal processing circuit which provides the weighed average versus difference during dual channel operation to give the CC-DLTS output of Equation (4.7).

To recapitulate the CC-DLTS technique, the experimental procedure involves first biasing a MNOS device into deep depletion or weak inversion. Superimposed on the dc bias is a charging pulse which drives the semiconductor surface into strong accumulation in order to populate the interface states with majority carriers. After the charging pulse, the gate voltage varies with time as the occupation of the interface states returns to its equilibrium distribution. The CC-DLTS signal, ΔV_g, is then obtained by forming the difference of the gate voltages measured at two delay times t_1 and t_2. The signal is measured in a temperature scan, and good noise discrimination is gained by time averaging over many cycles with a Boxcar averager.

5.3 The Analysis of the CC-DLTS Spectra

In an N-type MNOS capacitor, the DLTS signal arises from the emission of electrons from interface states in the upper half bandgap. Several qualitative features of CC-DLTS measurements on N-type MNOS capacitors are illustrated in Figure 5.4. This figure shows how CC-DLTS spectra vary with different reverse bias conditions under the same sampling time constant $t_2 = 2t_1 = 5$ msec. The first four curves are biased into depletion region, so that the Fermi

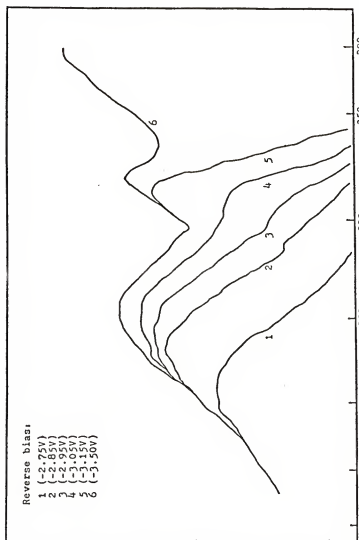


Figure 5.4 The CC-DLTS spectra for an N-type MNOS capacitor under different reverse bias conditions, sampling time $t_2 = 2t_1 = 5$ ms

level intersects the interface above the Si midgap. The fifth and sixth curves are measured when capacitor is biased into deep depletion such that the Fermi level is located below the midgap during reverse biasing.

Since ΔV_g is contributed from peak emission, as illustrated in Figure 4.4 and Figure 4.5, it is clear that the first curve in Figure 5.4 is due to the emission of electrons from part of the trap states located near the conduction band edge. As the amplitude of the reverse bias increases, ΔV_g becomes larger and covers a wider energy range. This implies that electrons are emitted from deeper trap levels as well. When reverse bias is greater than -3.15V, signal saturation is reached around room temperature. Therefore, ΔV_g can be adopted and corrected provided that the capacitor is biased far enough into depletion such that under equilibrium conditions the Fermi level intersects the interface states below midgap. In addition, the bias-dependent ΔV_g reveals that the interface between thermally-grown SiO_2 and Si possessing a continuous distribution of electronic trapping centers throughout the Si forbidden band edge. Above 300K, ΔV_g depends strongly on the depletion capacitance and increases rapidly as the device is biased further into depletion. The peak near 325K and the sharp increase in the signal at higher temperatures occur when the capacitor is biased into inversion region. It is ascribed to the onset of minority carrier emission and capture processes at the interface

states. The degree of increase depends on the surface bending condition. The larger the bias voltage, the larger the ΔV_g. To verify this situation, it is claimed that minority carrier emission occurs within the region between midgap and Fermi level. Right after the accumulation pulse, majority carrier emission presents at a higher emission rate. Later, hole emission occurs at a slower rate. The two emission processes are superimposed and are sampled by the Boxcar averager which gives the average difference of two sampled signals. An increase in ΔV_g is thus presented.

A comparson of the CC-DLTS and the DLTS signals for an N-type MNOS capacitor with time constants $t_2=2t_1=5$msec was performed with two different gate reverse bias voltages and the results are shown in Figures 5.5 and 5.6. In Figure 5.5, for $V_g=-3.2V$ (before strong inversion), it shows an immediate drop of ΔV_g and DLTS signal for T>325K. In Figure 5.6, $V_g=-3.5V$ (near strong inversion) ΔV_g increases continuously and the DLTS signal increases rapidly for T>350K. It implies that more hole emission is involved. When temperature rises above 380K, hole capture from the valence band to the peak hole trap in the lower half bandgap occurs. Consequently, the recombination between electron and hole may occur, which results in the drop of ΔV_g and the DLTS signal. A proper selection of bias is necessary to reduce bulk-trap interference [23] and to avoid the memory shift (i.e., change nitride charge)

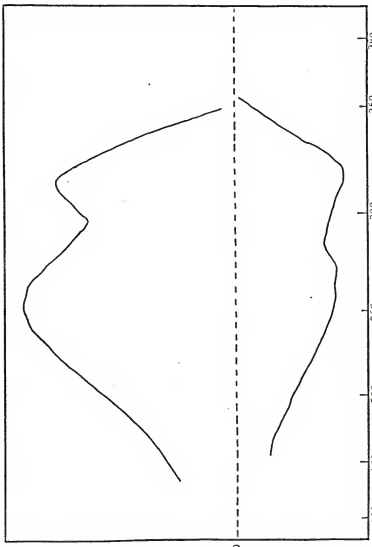


Figure 5.5 The CC-DLTS and DLTS scans for an N-type MNOS capacitor under weak inversion bias condition

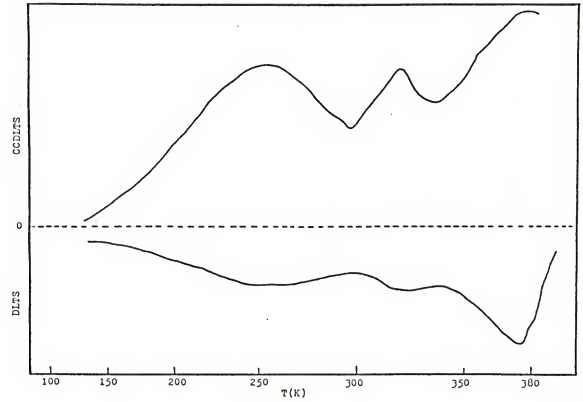


Figure 5.6 The CC-DLTS and DLTS scans for an N-type MNOS capacitor under strong inversion bias condition

during CC-DLTS measurements. Wang [23] demonstrated the different DLTS spectra resulted from improper bias condition. After a careful examination, we found that the DLTS spectra shown in Figure 5.5 resembled those of Wang's under accurate bias condition. Thus, his work supports our data.

The RF signal in the CC-DLTS technique plays an important role on driving dynamic emission signals and coupling it through the inductive transformer to amplification and demodulation. Therefore, the higher the frequency used in the experiment, the better the sensitivity that is obtained.

Additionally, one faces a trade off between signal-to-noise ratio on one hand and signal resolution on another in terms of the choice of drive level. Figure 5.7 illustrates the CC-DLTS measurement for two different RF frequencies, 10MHz and 20MHz, and the result shows that ΔV_g is independent of the RF signal frequency used.

Typical CC-DLTS spectra measured on an unexercised P^+-emitter gridded and an unexercised P^+-base gridded MNOS capacitor with t_1=10 msec and t_2=20 msec are shown in Figure 5.8. The result shows that there is no significant difference in the voltage transient between these two MNOS capacitors. The grids are diffused into N-substrate before Si_3N_4 layer deposition. The main function of this structure is to provide the write/erase cabability by means of supplying minority carriers (holes) via P^+-grids. The

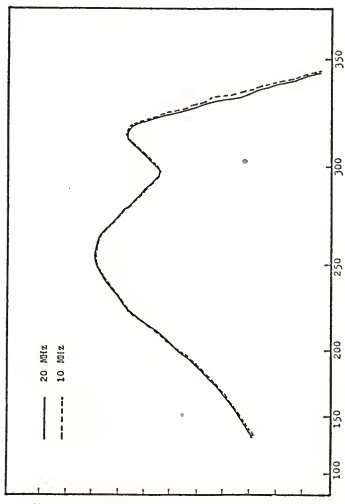


Figure 5.7 The frequency-independent property in the surface state measurements by using the CC-DLTS technique, where V_g = -3.2 volts, $t_2 = 2t_1$ = 5 ms

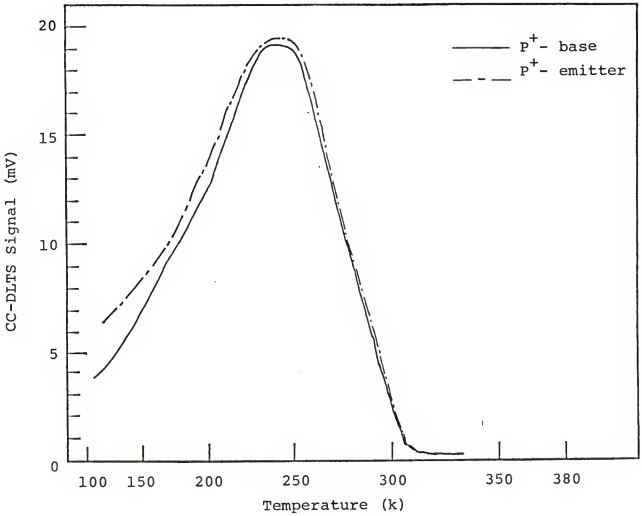


Figure 5.8 A comparison of the CC-DLTS thermal scans between a P^+-base gridded and a P^+-emitter grided MNOS capacitor, $t_2 = 2t_1 = 10$ ms

carrier transport response time is much faster than the generation rate of minority carriers in the space charge region and relaxation time in the N-type bulk silicon. Therefore, an inversion layer is presented on the surface right after the charging pulse while biasing into inversion, eliminating the problem of minority carrier generation at higher temperatures while using simple MNOS capacitor structure. Thus,the gridded structure eases the difficulty of calculating surface state density and energy distribution through the CC-DLTS spectra. Figure 5.8 indicates that no sharp increasing peaks occur at high temperatures, for the reason that the emission of electrons is contributed from the traps near midgap or below midgap at very high temperatures. Holes in the valence band recombine with electrons at interface recombination centers as soon as electrons are captured by the interface traps near midgap.

Both $N_{ss}(E)$ and E(T) were determined from the semi-empirical formulas as given in Equation (4.24) and (4.25). Figure 5.9 shows the $N_{ss}(E)$ vs energy in the upper half bandgap of silicon surface for two unexercised MNOS capacitors. It is shown that native surface states observed in the P^+-emitter gridded MNOS capacitor are similar to that of the P^+-base gridded MNOS capacitor with surface state density N_{ss} ranging from $2x10^{10}$ $cm^{-2}eV^{-1}$ to $1x10^{12}$ $cm^{-2}eV^{-1}$. A trap density peak is presented at 0.37eV below the conduction band edge and tends to drop slowly towards

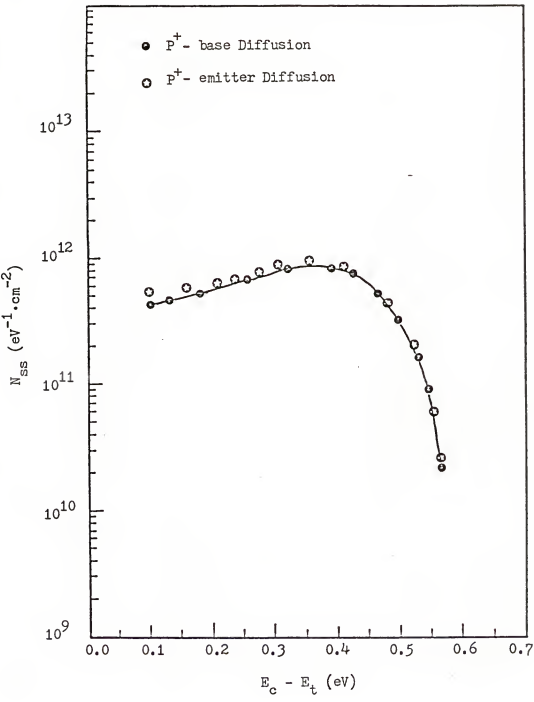


Figure 5.9 A comparison of the surface state densities in the upper half bandgap of an N-type substrate between the P^+-base and the P^+emitter gridded MNOS capacitors

E_c. No evidence of sharp increase in surface-state density near the band edge is found. Same phenomenon was observed by Berglund [57] in MNS devices, Uranwala et al. [22], and Wei and Simmons [58] in MNOS devices using different measurement techniques.

Figure 5.10 shows the CC-DLTS temperature scans (ΔV_g vs T) for four MNOS capacitors with different W/E cyclings. Devices under test were P^+-emitter gridded MNOS capacitors exercised under 30V pulse height, 1 μsec pulse width. These data are converted into surface state density vs energy relation, and the results are shown in Figure 5.11 along with the data of one MOS capacitor fabricated on <100> silicon substrate. The results clearly show that midgap interface state density increased drastically for W/E cycles exceeding $1x10^9$ cycles, while little change in the interface state density was observed for W/E cycles less than $1x10^7$. At $1x10^{10}$ W/E cycling, the midgap interface state density was increased by nearly two orders of magnitude over the unexercised device. From Figure 5.11, it is noted that the interface state density in an MNOS capacitor is in general higher than that of an MOS capacitor fabricated under identical processing conditions. It is noted that a 30 Volts exercise pulse seems to create more damage in SiO_2 layer due to the high electric field strength. However, it is possible that high series resistance in the silicon bulk will lower the voltage drop across the SiO_2 layer during high charging and discharging

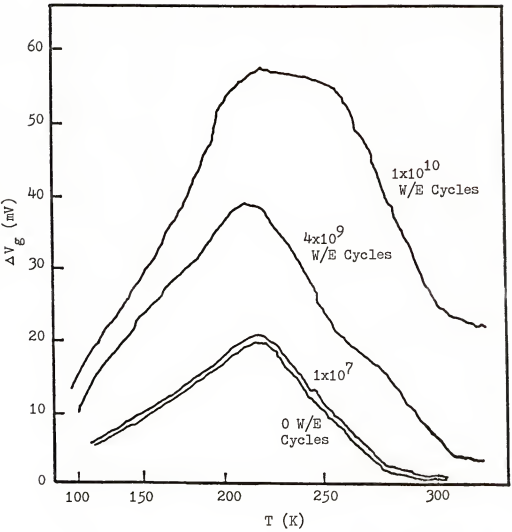


Figure 5.10 The CC-DLTS thermal scans for four P^+-emitter gridded MNOS capacitors exercised at 0, 10^7, $4x10^9$, and 10^{10} W/E cycles using a 30 Volt, 1 μsec pulse

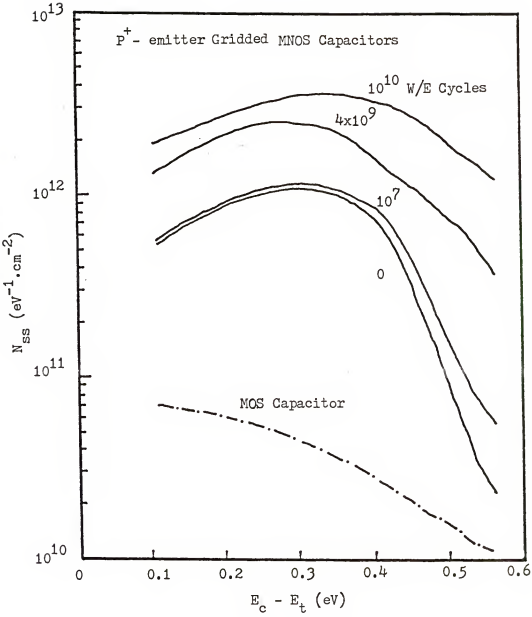


Figure 5.11 Interface state density vs energy in the band-gap for the four MNOS capacitors shown in Figure 5.10 and for one MOS capacitor, as calculated from the CC-DLTS method

transient periods. This may explain why this MNOS capacitor can hold up to $1x10^{10}$ W/E cycles.

Figure 5.12 shows the interface state density vs energy curves for three MNOS capacitors exercised at 0, 10^8,$5x10^9$ W/E cycles by using a 26 Volts, 10μsec pulse. For these P^+-gridded capacitors, the doping concentration of the P^+ grids is $5x10^{18}$ cm^{-3} and the resistivity of N-substrate is 3-5 ohm-cm. In the 1410 mask series samples, the grid spacing is equal to 75 μm and grid width is 5 μm. Results show a significant increase of surface state densities due to prolonged cycling. In addition to the broadening in the interface state shape, the interface state density near midgap also shows a drastic increase. The peak density reaches $5.8x10^{12}$ $cm^{-2}eV^{-1}$ after $5x10^9$ W/E cycling.

5.4 Discussion

It is important to know how deep the interface states are located from the Si-SiO_2 interface into the SiO_2 layer. Preier [59] calculated the interface state density in the MOS capacitor from the admittance measurements by assuming that interface states were distributed into the oxide and were charged and discharged by tunneling. Nicollian and Goetzberger [60] found that interface states were located within 10Å of the Si-SiO_2 interface to obtain a good fit to the admittance measurements. Using photo I-V method and C-

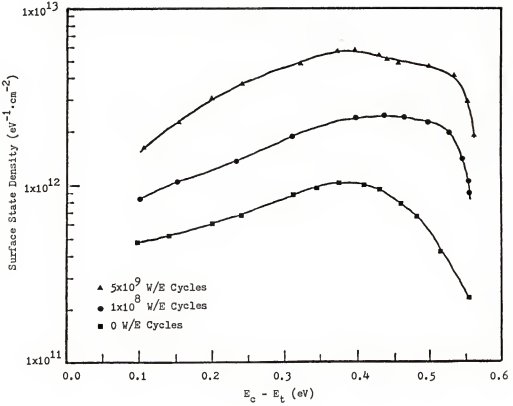


Figure 5.12 The surface state density vs energy after W/E prolonged cyclings measured on emitter gridded MNOS capacitor with 26 volts, 10 μsec pulse

V measurement [61-62], it was found that oxide fixed charge density is about $5x10^{11}$ cm^{-2} and 90% of these electrically active centers were located within 34Å of the interface. By photo thermal probing of the Si-SiO_2 interface [63], it was suggested that oxide fixed charges have energy levels outside the silicon bandgap. Therefore, their occupancy can not be changed with gate bias since Fermi-level can be varied only within the bandgap. Nevertheless, for atomically similar centers, oxide fixed charges may be regarded as active centers located in the oxide deeper than interface states since the time constants of charge exchange between these active centers and silicon bulk are so long that they could be treated as nonvolatile charge centers.

In studying the chemical composition and width of the interface, it has been shown that a transitional region of nonstoichiometric oxide exists at the Si-SiO_2 interface. However, its width tends to vary roughly in proportion to the depth resolution of the method used. The width was found to be 20Å from low energy ion backscattering experiment[64]; 6-35 Å from Auger electron spectroscopy [65]; 5-20 Å from X-ray photoelectron spectroscopy [66]. Thus, the interfacial layer or the location of the electrically active centers is no wider than about 30Å. Grunthaner et al. [67] proposed an appealing picture of the Si-SiO_2 interface; i.e., the interfacial region is comprised of a single-crystal silicon layer followed by (1)

a monolayer of incompletely oxidized silicon, (2) a strained region of SiO_2 roughly 10-40 Å deep, and (3) the remaining stoichiometrical, strain free amorphous SiO_2.

In this study, a defect model is adopted to explain the degradation mechanisms of the interface states. Generally, four types of defects could exist at or near Si-SiO_2 interface; they are (1) excess silicon (trivalent silicon [68]), (2) excess oxygen [69] (nonbridging oxygen), (3) impurities [59], and (4) states in oxide charge induced potential wells [70].

For the trivalent silicon atoms, they are probably related to the incomplete oxidation of silicon or to the generation of vacancies in silicon during oxidation. The fourth unsatisfied valence bond may act as a hole trap. After capturing a hole, it becomes positively charged and remains neutral when it is empty. Nonbridging oxygen is defined when one of the Si-O bonds is broken. Its unsatisfied valence bond acts as an electron trap. After electron capture, it becomes negatively charged and remains neutral when it is empty. According to their individual properties described above, trivalent silicon can be treated as a donor type interface state while nonbridging oxygen is treated as acceptor type interface states. The most satisfactory model for explaining the surface states behavior at Si-SiO_2 interface was proposed by Gray and Brown [71] for unirradiated MOS devices; this model has received wide support from many researchers [72-

75]. The model assumed that the interface states in the upper half bandgap are acceptor type states and those in the lower half are donor type states. The charged acceptor states would cause a positive shift on C-V curve and the charged donor states would cause a negative shift.

Stein et al. [76] used the Sputter Auger Electron Spectroscopy (SAES) technique to characterize the defects in $Si_3N_4/SiO_2/Si$ structure, in which they reported that nitride atoms were penetrated into thin oxide layer during high temperature Si_3N_4 deposition. The pileup of nitride at $Si-SiO_2$ interface may contribute to the high surface state density in the MNOS structure.

Results shown in section 5.3 indicate that the creation of fast surface state N_{ss} is due to prolonged W/E cycling. The broadened "U" shape and the voltage shift in CV curve also reveal the generation of N_{ss} owing to high W/E cycles.

Since the SiO_2 layer is as thin as 20Å, the transition region, which consists of fast surface states, slow surface states, and fixed charge memory states, is the major portion of this layer. The original bonding among atoms is weak. Large excitation force, such as repeated high electric field strength crossing this layer with field strengths greater than 10^6 V/cm during W/E exercise, can easily break the Si-Si or Si-O-Si bonding. Consequently, more trivalent silicon and nonbridging oxygen are presented in the silicon dioxide layer. The new defects generated

will cause the dielectric fatigue, threshold voltage shift, short endurance, and retention loss.

The CC-DLTS technique has been demonstrated as a powerful tool for study of the surface states on an MNOS structure. It provides ability for quantitative analysis of the surface states on exercised MNOS devices. Detailed calculations of threshold voltage shift and the interpretation of MNOS failure mechanisms will be given in Chapter VI for P^+-gridded MNOS capacitors.

CHAPTER VI
ANALYSIS OF A P^+-GRIDDED MNOS CAPACITOR

6.1 Introduction

The information of surface states near the oxide-silicon interface can be obtained by comparing the shift between the theoretical and the experimental C-V curve of an MIS structure. The scope of the C-V technique, however, is limited by the inability of minority carrier generation to follow the change of ac signals at highfrequencies, thus prohibiting the comparison of theoretical and experimental C-V curves at these frequencies. The gridded MIS structure is proposed to facilitate this comparison by increasing the availability of minority carriers in the inversion layer, thereby permitting the MIS capacitor to possess quasi-static high frequency characterization at 1MHz [77].

To evaluate the influence of specified processing variables on the dynamic properties of an MNOS device (i.e., switching speed, window width dependence upon pulsed biasing), an FET configuration is usually required for the reason that write and erase could involve the motion of both electrons and holes. The use of FET structure for these studies is undesirable due to the complication

involving in multiple masking. Since undoped wafers will show high speed charge transfer only for the majority carriers, a simpler approach is embodied in the use of "gridded" MNOS structures. For the case of P-channel devices, a rectangular grid of P^+ diffusion is used on the 3-5 ohm-cm N type silicon substrate. The gridded structure requires only one masking step, as compared to five for FET's.

The use of the gridded structure enables high speed write/erase programming with pulse width even below one microsecond. Since the bias voltage at the minimum corresponds approximately to the threshold voltage of the equivalent FET's, the use of the shift of the minimum (V_{min}) could be a simpler index for measuring charge window width than referring the flat band voltage shifts with non-gridded structures. Additionally, the generation of $Si-SiO_2$ interface fast states owing to high stress write/erase cyclings is indicated by the widening of the "U" shape on the C-V traces. A good correlation between interface states and write/erase cycling will be discussed.

The results presented in this chapter are focussed on explaining the HFCV characteristics as well as carrier transport mechanisms of an P^+-gridded MNOS capacitor. Device fabrication will be given in Section 6.2. Detailed equivalent circuit will be given in Section 6.3. Section 6.4 gives the comparison of theoretical and experimental data. The conclusion is given in Section 6.5.

6.2 Device Fabrication

To facilitate the exercising purpose of the MNOS capacitors, "gridded" silicon wafers were used as substrates for the test capacitors. Fabrication of these capacitors began by assembling a group of N-type, 3-5 ohm-cm, and [100] orientation, silicon wafers into a wafer lot for processing. First, an oxide was grown on the wafers to a 5000Å thickness in steam at 1100 °C. Next, a grid pattern was etched into the oxide, exercising the underlying silicon. The grids comprise horizontal and vertical bars of 5 micron width with 75 micron center to center spacing. Boron was deposited on the wafers using the standard thermal diffusion procedure, and the etched oxide was regrown in a 900 °C, 90 minutes steam process. At this point, two processing options were available. One option was to strip all oxide from a wafer, deposit the MNOS dielectric, and then deposit aluminum capacitor dots through a shadow mask in the metallization system. The other option was to pattern and etch the oxide, using a mask which defined areas for MNOS capacitors of various sizes. The MNOS dielectric was next deposited, followed by a standard aluminum deposition, metallizing the entire wafer. The aluminum was next patterned and etched by a mask which defined the capacitors and small probe pads. The contact pads are extended from the capacitors to outer edge

over the initial thick oxide. The top view and side view of a gridded MNOS capacitor are shown in Figure 6.1.

The virtues of processing by the second option are that edge effect around the capacitor is minimized, the capacitor is of uniform size across a wafer, and no mechanical connection has to be made to the capacitor itself. The latter virtue eliminate stress effects, anomalously shorted devices, and premature catastrophic breakdown during endurance testing.

The resulting substrate structure fabricated by the process could provide both majority and minority carriers for injection into the MNOS dielectric. This allows the writing and erasing of a test capacitor with pulse lengths comparable to those used for programming MNOS transistors on the order of microseconds. In turn, this programmability made possible the endurance testing of capacitors. As very little processing was required to generate test capacitors once the MNOS dielectric had been deposited, the practice of using gridded pilot wafers in each MNOS dielectric deposition lot and quickly characterizing them had the potential for being an excellent process control procedure for the fabrication of MNOS transistors.

6.3 The Equivalent Circuit for the Gridded MNOS Capacitor

The purpose of using the gridded MNOS structure is to enable us to perform the writing and erasing tests and to

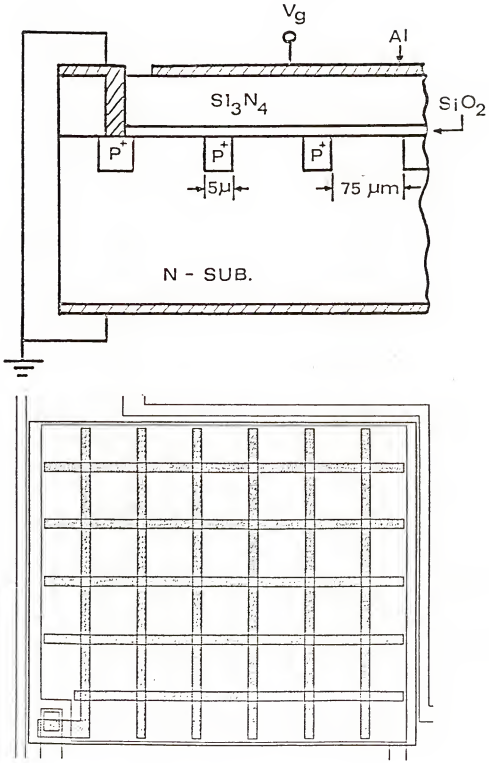


Figure 6.1 The example of P^+-gridded N-type MNOS capacitor structure (a) side view, (b) top view

present Quasi-static high frequency C-V characteristics at 1MHz. Since the contribution of the interface states to the capacitance tends to be zero at high frequencies [78], the interface states effect above 1MHz in this equivalent circuit modeling is neglected.

In the P^+-gridded MNOS capacitor structure shown in Figure 6.1, the N-type dopant density on the substrate is about $2x10^{15}$ cm^{-3}, and the P^+-diffusion grid pattern is heavily doped. For example, for the emitter diffusion case, the boron dopant concentration is $1x10^{20}$ cm^{-3}, and for the base diffusion process, it is $5x10^{18}$ cm^{-3}. The diffused regions are treated as many small P-type MNOS capacitors while the N-type surface portion are treated as mainly N-type MNOS capacitors. The voltage scan is performed for the N-type capacitor from strong accumulation region through depletion region into strong inversion region, while for the P-type capacitor, the scan is in the opposite direction. Therefore, an assumption is made that the total P-type capacitance maintains the same value as the insulating capacitance during the C-V measurement. The total insulating capacitance, C_I, is the sum of series capacitance of the nitride and oxide insulators.

Analysis is made for uniform doping concentration only. Although nonuniform doping profiles result from ion inplantation or from impurity redistribution during oxidation may exist, the uniform case is of such major importance that it warrants detailed discussion.

In the accumulation and depletion regions, the equivalent circuit is given in Figure 6.2, where C_I is the insulating capacitance per unit area; C_S represents the space charge capacitance per unit area; R_s is the series resistance exists between the substrate contact and the silicon surface; R_p is the effective resistance of P^+-grid, and A_p and A_n stand for the area of gate metal under P^+-grid and N-substrate region, respectively. The P^+-grid is electrically tied to the substrate contact. The capacitance in P^+-grid region, C_{IP}, is contributed from the hole exchange while applying ac small signal on the gate. The hole (majority carriers in this area) is replenished from external source through Ohmic contact to the surface of P^+-region.

In the weak inversion and strong inversion regions, the minority carrier generation in the N-type depletion region can not follow the ac signal at high frequencies. However, the inversion layer and P^+-grid form a high-low P^+-P junction. The lateral P^+-grid supplies holes to the inversion layer while DC bias vertically applied to the P^+-P structure is in thermal equilibrium condition. No current flows in the horizontal direction. If a small ac signal superimposed on DC bias, the N-type surface will no longer be in equilibrium. A constant surface potential on P^+-grid surface is assumed when the amplitude of the ac signal is less than kT. The carrier transport between the P^+-P high-low junction is presented in terms of channel

resistance, R_N, which is in series with the channel capacitance, C_{CN}. The series relation is based on the fact that these elements represent the flow and charge-up of the same carriers originated from the same source (i.e., holes flow from the inversion layer into the diffused grids and vise versa). The frequency response of the MNOS device is determined by the RC time constant. Thus, the area between grids (which define the channel resistance R_N or the channel conductance G_N) and R_P contribute the value of R. The space charge capacitance C_S, associated with the channel capacitance, contributes to the total differential capacitance on the N-type surface. The equivalent circuit in the inversion region is shown in Figure 6.3 where the effective resistance of the P^+ grids, R_P, is also included.

The total input admittance of the MNOS capacitor can be represented by the total conductance G_T and the total capacitance, C_T,

$$Y_{in} = G_T + jwC_T \tag{6.1}$$

where

$$C_T = (A/D_1) + (B/D_2) \tag{6.1a}$$

$$C_T = (C/D_1) + (D/D_2) \tag{6.1b}$$

$$C_{IP} = C_I A_P \tag{6.1c}$$

$$C_{IN} = C_I A_N \tag{6.1d}$$

$$C_{SC} = C_S A_N \tag{6.1e}$$

$$A = w^2 C_{IP}^2 R_P + w^4 C_{IP}^2 C_{JP}^2 R_S R_P (R_S + R_P) \tag{6.1f}$$

$$B = w^4 C_{IN}^2 \{C_{SC}^2 R_S + C_{CN}^2 (R_N + R_P)\} + w^6 C_{IN}^2 C_{SC}^2 C_{CN}^2 R_S (R_N + R_P)(R_S + R_N + R_P) \tag{6.1g}$$

$$C = C_{IP} + w^2 C_{IP} C_{JP} \{C_{JP}(R_P + R_S) + C_{IP} R_P^2\} \tag{6.1h}$$

$$D = w^2 C_{IN}(C_{SC} + C_{CN})(C_{IN} + C_{SC} + C_{CN}) + w^4 C_{IN} C_{SC} C_{CN} \{C_{SC} C_{CN}(R_S + R_N + R_P)^2 + C_{IN} C_{CN}(R_N + R_P)^2 + C_{IN} C_{SC} R_S^2\} \tag{6.1i}$$

$$D_1 = 1 + w^2 \{2 C_{IP} C_{JP} R_P^2 + C_{JP}^2 (R_P + R_S)^2 + (C_{IP} R_P)^2\} + w^4 C_{IP}^2 C_{JP}^2 R_S^2 R_P^2 \tag{6.1j}$$

$$D_2 = w^2 \{2 C_{IN}(C_{SC} + C_{CN}) + C_{IN}^2 + (C_{SC} + C_{CN})^2\} + w^4 \{(C_{SC} C_{CN} R_S)^2 + 2(C_{SC} C_{CN})^2 R_S (R_N + R_P) + [C_{SC} C_{CN}(R_N + R_P)]^2 + (C_{IN} C_{SC} R_S)^2 + [C_{IN} C_{CN}(R_N + R_P)]^2 + 2 C_{IN} C_{CN} C_{SC}^2 R_S^2 + 2 C_{IN} C_{SC} C_{CN}^2 (R_P + R_N)^2\} + w^6 \{C_{IN} C_{SC} C_{CN} R_S (R_N + R_P)^2\} \tag{6.1k}$$

To characterize the high-frequency C-V, C_T is considered important and can be calculated from Equation (6.1b). To be precise, the junction capacitance between P-

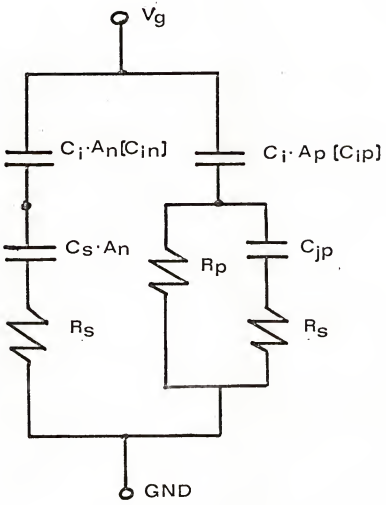


Figure 6.2 The equivalent circuit for P^+-gridded MNOS capacitor which is biased into accumulation and depletion region

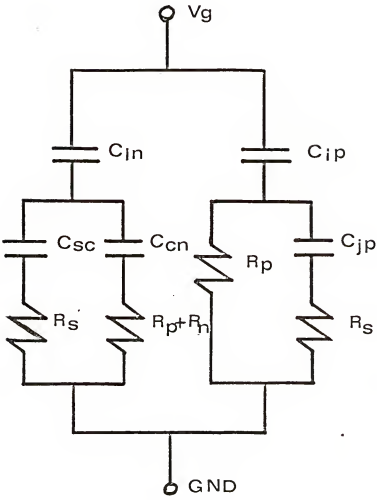


Figure 6.3 The equivalent circuit for P^+-gridded MNOS capacitor under inversion region

grid and N-substrate, the sheet resistance effect, the resistivity of P^+-grid, and the effective hole mobility in the inverted channel are taken into consideration in this modeling.

In order to correlate the "U" shape in the C-V curves with the degradation of an exercised MNOS device, analysis of the CC-DLTS experiment data will be given in Section 6.4.

6.4 The Parameters in Equivalent Circuit

6.4.1 Space charge capacitance, channel capacitance and the resistivity of grids

Using Poisson equation, charge neutrality condition and Gauss law, we obtain relationships among thesurface electric field, E_s, surface charge density, Q_s, and the surface band bending for an MNOS capacitor.

$$E_s = \pm\left(\frac{\sqrt{2}\ kT}{qL_D}\right)\{e^{U_s} - U_s - 1) + e^{-2U_B}(e^{-U_s} + U_s - 1)\}^{1/2} \quad (6.2)$$

$$Q_s = \mp\left(\frac{\sqrt{2}\ \varepsilon_s kT}{qL_D}\right)\{e^{U_s} - U_s - 1) + e^{-U_B}(e^{-U_s} + U_s - 1)\}^{1/2} \quad (6.3)$$

where U_s is normalized surface potential

$$U_s \triangleq \beta\psi_s$$

Use negative sign for $\psi_s > 0$ and positive sign for $\psi_s < 0$.

The space charge capacitance per unit area is given by

$$C_s \triangleq -\frac{\partial Q_s}{\partial \psi_s}$$

$$= \pm \frac{\varepsilon_s}{\sqrt{2}\, L_D} \{ \frac{(e^{U_s} - 1) + e^{-2U_B}(1 - e^{-U_s})}{F(U_s, U_B)} \} \qquad (6.4)$$

where $L_D = (\varepsilon_s kT/q^2 N_D)^{1/2}$ is the Debye lengthand

$$F(U_s, U_B) = \{ e^{U_s} - U_s - 1) + e^{-2U_B}(e^{-U_s} + U_s - 1) \}^{1/2}$$

Under flat band condition, $\psi_s = \emptyset$, and

$$C_S(\psi_S) = \varepsilon_s / L_D \qquad (6.5)$$

Equation (6.4) holds for any frequencies under equilibrium condition. The total charge, Q_s, includes both free electrons and holes in the space charge region.

At sufficiently high frequencies, the inversion charge can not follow the ac signal. Hence, C_S becomes

$$C_s(U_s) = \frac{\varepsilon_s}{\sqrt{2}\, L_D} \frac{(e^{U_s} - 1)}{(e^{U_s} - U_s - 1)^{1/2}} \qquad (6.6)$$

The quasi-static C-V curve [see Equation (6.4)] and the high frequency C-V curve [Equation (6.6)] are plotted in Figure 6.4.

In the inversion region ($U_s < -U_B$), holes transport between the P^+-grides and the inversion layer are defined

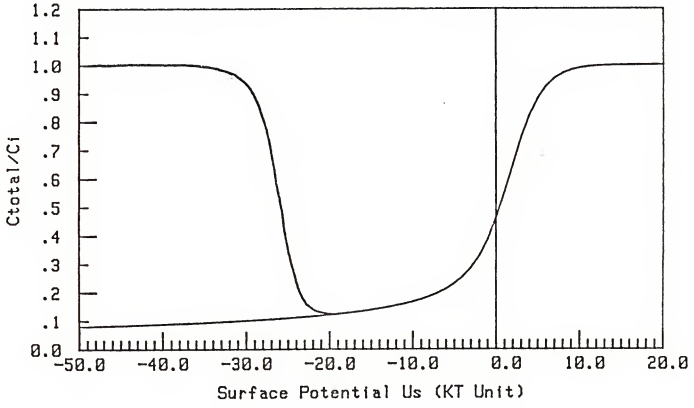


Figure 6.4 Standard quasi-static calculated CV and measured CV at 1 MHz vs surface potential for an N-substrate MNOS capacitor with $2x10^{15}$ cm^{-3} doping density

by the sheet resistance on the P^+-side, and the channel resistance R_N in the inversion channel.

Varying doping concentration of grid pattern with different masking processes leads to different R_p. For Harris 1410 mask series, the grid spacing is 75μm and the grid width is 5μm, while in 1338 mask series, it is 37.7μm and 7.5μm, respectively. For P^+-emitter diffusion, the doping concentration is $1x10^{20}$ cm^{-3}, and the resistivity is equal to $1.2x10^{-3}$ ohm-cm [79]. The junction depth is approximately 1μm. For P^+-base diffusion, the doping concentration is $5x10^{18}$ cm^{-3}, and the resistivity is equal to $1.4x10^{-2}$ ohm-cm; the junction depth is about 1.8μm. Through simple calculation, the sheet resistance of the emitter grids is 12 ohm/square, and the sheet resistance for the base grids is 77 ohm/square. The top view of grid structure is shown in Figure 6.1a.

Calculating the average length $\langle L_{eff} \rangle$ from Ohmic contact to the opposite corner of the MNOS capacitor, the grid area is around $7.2x10^{-4}$ cm^2; dividing this grid area by grid width one obtains 97.5 squares of the resistivity for 1410 mask and 54.5 squares of the resistivity for the 1338 mask. Thus, values for R_p are given respectively by

$R_p = 1.170K\Omega$ for # 1410, P^+-emitter grids

$R_p = 7.507K\Omega$ for # 1410, P^+-base grids

and

$R_p = 654\Omega$ for # 1338, P^+-emitter grids

R_p = 4.19KΩ for # 1338, P^+-base grids

For MNOS capacitors with area larger than 7.2×10^{-4} cm^2, values of R_p will increase as well. This is the case for those MNOS capacitors with 200 pF or 500 pF capacitances. The R_p changes approximately linearlywith the size of the capacitor.

In strong inversion region, the charge due to minority carriers within the inversion layer, Q_p, can be obtained by

$$Q_p = Q_S - Q_B \tag{6.7}$$

where

$$Q_B = \sqrt{2} q N_D L_D \{e^{U_s} - U_s - 1\}^{1/2} \tag{6.7a}$$

and the channel capacitance per unit area is denoted as

$$C_c = \frac{\varepsilon_s}{\sqrt{2}\, L_D} \left\{ \frac{-[(e^{U_s} - 1) + e^{-2U_B}(-e^{-U_s} + 1)]}{F(U_s, U_B)} + \frac{(e^{U_s} - 1)}{(e^{U_s} - U_s - 1)^{1/2}} \right\} \tag{6.8}$$

The channel conductivity can be approximated by

$$\sigma(x) = q p_n(x) \mu_p(x) \tag{6.9}$$

and the channel conductance is then given by

$$g_c = \frac{Z}{L_c} \int_0^{x_i} \sigma(x)\,dx \tag{6.10}$$

where Z is the channel width, and L_c is the channel length. For constant effective hole mobility, μ_{eff}, the channel conductance becomes

$$g_c = \frac{qZ\mu_{eff}}{L_c} \int_0^{x_i} P_n(x)\,dx$$

$$= \frac{Z}{L_c}\,\mu_{eff}\,Q_p \tag{6.11}$$

For a small perturbation on the inverted surface, Q_p is assumed independent of surface position in equilibrium. Therefore, the channel resistance R_N along the channel is equal to

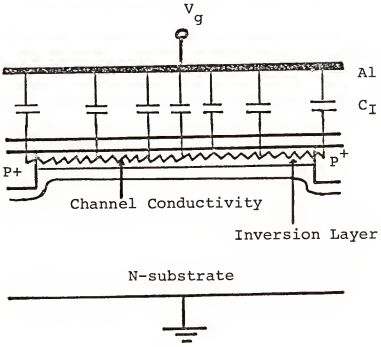
$$R_N = \frac{L_c}{Z\,\mu_{eff} Q_p} \tag{6.12}$$

Since hole relaxation in a gridded MNOS capacitor due to ac signal is a two dimensional problem, L_c/Z can not be treated as in the case of MOSFET device. In order to find the value of L_c/Z, a unit grid capacitor is used which contains 2.5μm-wide grids on four sides of an N-type capacitor with 70μm squares of area in the center.

The steady state quasi-equilibrium condition will be considered if the hole relaxation onto any point of the N-

type inversion surface responds to high frequency. Then, the measured capacitance will be equal to the insulating capacitance C_I. If the frequency is too high so that there are some portions of the surface which can not be replenished by holes from the P^+ region, the total capacitance will be less than C_I. The time constant defined by $R_N C_{CN}$ product determines the frequency response. From this respect, we may conceive that the unit grid capacitor consists of many RC networks (C is in the vertical direction from gate to surface; R is distributed in the horizontal direction over the whole inversion layer) which delay the carrier charging or discharging process, as shown in Figure 6.5(a). The grid capacitor is divided into nine squares with equal size as appears in Figure 6.5(b). The center square can be treated as pure capacitor. When the charge is injected at the center point of the capacitor, it will immediately spread over this square; its time delay is near zero. There are four squares jointed to the center square like pure resistors, and thus the charges at the center point will take time (RC effect) to reach the P^+-grids via the closest routes. The last four squares on the corners are conceived as a combination of capacitive and resistive elements. The charges that flow through these areas will take a longer time to reach P^+ grids. However, their contribution to the channel conductivity can be approximated as one square in all. Thus, even though there is only one square of channel conductance in every

(a)



(b)

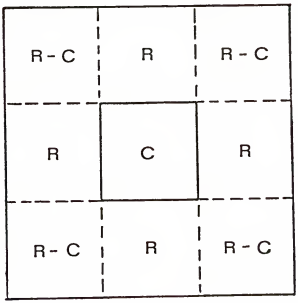


Figure 6.5 The approximation of the number of squares of the effective channel conductivity (a) charge injection from the center of the gate plate through RC network, (b) the grid capacitor is divided into nine squares with equal size under inversion condition

direction that is perpendicular to side grids, there are four times more of routes for charge conduction. In addition to this, one square of conductivity contributes from regions on the corner. Finally, the two dimensional charge flow problem is solved by approximating the value of L_c/Z to 1/5. Thus, we have

$$R_n = \frac{1}{5\ \mu_{eff} Q_p} \tag{6.13}$$

where μ_{eff} is the effective channel mobility in the P-inversion layer, which will be discussed next.

6.4.2 Channel mobility

Mobility is an important parameter that reflects carrier transport properties in semiconductors. In a MOSFET structure, the strong gate field confines carriers to a very thin channel. This is in contrast to the transport mechanism in a bulk semiconductor. The thin channel, for instance, causes quantization effects and conductance anomalies [80-84]. The magnitude of low field mobility in the channel is smaller than in the bulk at room temperature. Over the last decade there have been extensive studies of the different surface scattering of carriers in terms of interface properties [85-88]. A brief review of some aspects of this work will facilitate the discussion of experimental results to be presented later in this and the next chapter.

In general, at least three different scattering mechanisms have been proposed to account for the mobility behavior in the region where the gate voltage is above threshold. Phonon scattering is important at room temperature [86], Coulombic scattering due to charge centers including fixed oxide charge Q_f, surface-state charge Q_{ss}, and localized charge due to ionized impurities Q_B [85-86]. The effects of Coulombic scattering are important for weakly inverted surfaces. High surface-charge densities or high substrate doping concentration will increase the Coulombic scattering. This type of scattering becomes less effective for a strong inverted surface because of carrier screening. Surface roughness scattering due to the asperities at the Si/SiO_2 interface [87-88] is important under strog inversion conditions.

The relative importance of these scattering mechanisms depends on the operating temperature as well as the strength of the surface electric field. At room temperature, the mobility is governed by the Coulombic scattering (due to charge centers) and the phonon scatterings in the low field region. In the weak-inversion (subthreshold) region, fluctuations of minority-carrier density generating by interface states and fixed oxide charges, have been proposed to account for mobility variations [89].

Recently, a new concept concerning mobility reduction with the transverse gate electric field has been introduced

[90-91]. The dependence of the mobility on this field is described by the "effective" field E_{eff}. The effective field E_{eff} is defined as

$$E_{eff} = \frac{1}{\varepsilon_s} [Q_b + \frac{1}{2} Q_{in}] \tag{6.14}$$

where Q_b is the space charge in the depletion region per unit area and Q_{in} is the induced mobile charge in the inversion layer. Sun and Plummer [91] and Baccarani and Wordeman [92] gave the effective mobility, μ_{eff}, an expression of the form

$$\mu_{eff} = CE_{eff}^{-1/n} \tag{6.15}$$

where C is an adjustable constant, and n is a parameter whose value varies between 3 and 5. Note that if the effective electric field is less than $2x10^5$ V/cm, then Equation (6.15) can not be used to describe the μ_{eff}. Tanimoto and Ferry[93] recently proposed a gate-field-induced carrier heating for μ_{eff}. Their empirical expression is given by

$$\mu_{eff} = \frac{\mu_o}{(1 + BE_{eff})^{1/2}} \tag{6.16}$$

when μ_o is the effective mobility at low field, and B is equal to $7.0x10^{-6}$ cm/V for the enhancement mode device,

4.8×10^{-6} cm/V for the depletion mode device. Although each author has stressed on different parameters, it is found that the behavior of Equation (6.16) fits the data given in references [90] and [91] in a range. They concluded that when substrate doping concentration is less than 1.0×10^{17} cm^{-3}, the effect of substrate impurity charge on effective mobility is not significant. The mobility reduction from fixed charge Q_f (10^{11} cm^{-2}) is interpreted as Coulombic scattering mechanism. The decrease of channel mobility by the transverse electric field is suggested by the presence of carrier heating.

The value of electron mobility for an MNOS structure was first reported by Hezel and Jager [94]. The effective electron mobility μ_{eff} was determined as a function of positive nitride charge density Q_N/q up to values of 10^{13} cm^{-2}. Special low-temperature-processed MNOS transistors with MIS contacts for source and drain were used for the measurements. Values of μ_{eff} for P^+-silicon were ranging from 100 to 400 cm^2/Vs, depending on Q_N and surface preparation. At high density of Q_N (7.5×10^{12} cm^{-2}) at the nitride oxide interface, μ_{eff} reduces to approximately 250 cm^2/Vs which is only 16.7% of the bulk mobility. It is surprising that their experimental data revealed such a low mobility in the inversion layer of the unexercised MNOS transistors.

It is interesting to note that a sever mobility degradation can occur after a prolonged W/E cycling, and

thus the model used for the MIS circuit design need to be modified for the MNOS circuit design.

To accurately explore the inversion layer mobility in an MNOS structure, an MNOS transistor structure should be used. In this study, a P^+-gridded MNOS capacitor structure is adopted to investigate the interface properties and to correlate the failure mechanisms for our MNOS memory devices.

6.5 Characterization of P^+-Cridded MNOS Capacitor by High Frequency Capacitance-Voltage (HFCV) Measurements

6.5.1 The HFCV method

The depletion layer charge density, the electron and hole densities, and the band bending in the silicon substrate of an MNOS capacitor were determined as a function of gate bias. The C-V characteristics reveal the response of both majority and minority carriers to the ac gate voltage. Majority carriers respond instantaneously to the ac gate voltage. In accumulation region, and in the depletion edge, the response time is in the order of a picosecond while in the depletion region near the interface, the response time is about a microsecond depending on the density of majority carriers. The minority carrier response is usually much slower ($>10^{-6}$ sec), and is important mainly in the inversion region. When the frequency of ac signal is greater than 1MHz, the

minority carriers are in nonequilibrium condition (see Figure 6.4). However, minority carriers can follow ac signal frequencies in the MHz range in some degree when a P^+-gridded MNOS structure is used. This mechanism will be discussed in sections 6.3 and 6.4. A comparison of the normalized capacitances in terms of surface potential is shown in Figure 6.6. In this figure, curve 1 is the capacitance measured on non-gridded capacitor structure at 1MHz, trace 2 is the theoretical high frequency capacitance (i.e. the Quasi-Static HFCV), trace 3 is the P^+-gridded capacitor at 1MHz with $2x10^{15}$ cm^{-3} N-substrate doping density and $1x10^{20} cm^{-3}$ P^+-diffusion grids.

Comparing the theoretical C-V curves of the normal MNOS and the P^+-gridded capacitors, the gridded capacitor possesses wider "U" shape due to the delay of hole transport between the P^+ grid and the inversion layer, and higher capacitance minimum C_{min} which is ascribed to grid effect. It is noted that the judgement of flatband point, weak inversion, and strong inversion regions on gridded capacitor becomes different from non-gridded structure. In this case, the threshold voltage is closed to $V(C_{min})$. This provides the convenience for calculating the amount of change in nitride charge by the write/erase pulses and a good estimation of the threshold voltage shift ΔV_T from prolonged W/E cycling. Varying P^+-grid geometry and parameter such as grid spacing L_S ,grid width L_W, and P^+ grids concentration N_A, will alter the HFCV

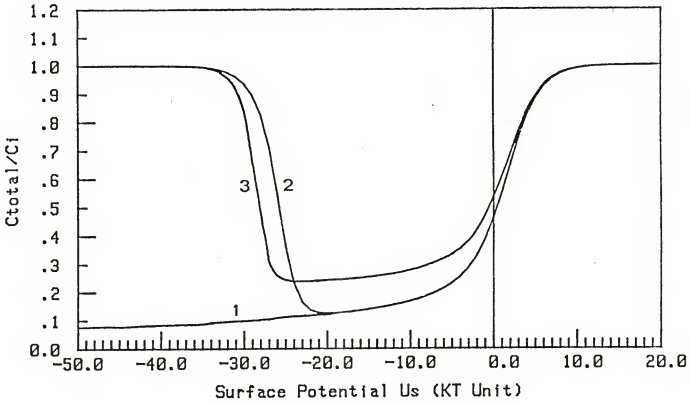


Figure 6.6 Normalized capacitance vs surface potential curves, curve 1 is the measured capacitance at 1 MHz on nongridded structure, curve 2 is the theoretic high frequency capacitance on nongridded structure, curve 3 is the measured capacitance on emitter gridded structure at 1 MHz in 1410 mask series

characteristics. Figure 6.7 illustrates three capacitance vs surfacepotentials for the P^+-base-gridded MNOS capacitors. Curve 1 is P^+-emitter gridded with L_s=38 μm and L_w=7.6 μm; curve 2 is P^+-emitter gridded with L_s=75 μm and L_w=5 μm; and curve 3 is P^+-base gridded with L_s=75 μm and L_w=5 μm. From this figure, it is shown that the P^+-grid area will determine the value of C_{min} and the width of "U" shape. In addition, the doping concentration of the diffused grids will affect the carrier transport time in the inversion region of the C-V curve.

The measured high frequency capacitance vs gate voltages for four different frequencies (i.e. 1MHz, 10MHz, 15MHz and 20MHz) on an N-type MNOS capacitor are plotted in Figure 6.8. Without P^+-grid, the behavior of the HFCV is similar to the MIS structure. However, the sheet resistance effect in the accumulation region and depletion region is so large that the capacitance depends strongly on frequency. Series resistance R_s may result in a serious error in the extraction of interface parameters and doping profiles from the admittance measurements. It can also limit the sensitivity of the small-signal steady-state methods. To avoid the error and sensitivity limitations, it is necessary to correct the measured admittance. However, due to the complexity of the gridded MNOS structure, it is not always possible to obtain an accurate estimation of R_s from the measured admittance in the strong accumulation region.

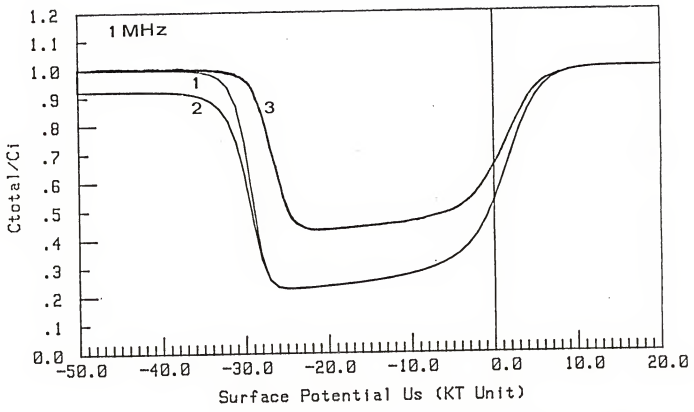


Figure 6.7 Curve 1 is the capacitance on 1410 P^+-emitter gridded MNOS capacitor, curve 2 is that on 1410 P^+-base series, and curve 3 is that on 1338 P^+-emitter series

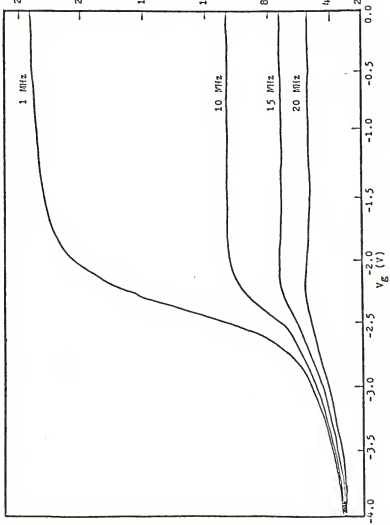


Figure 6.8 The series resistance effect on high-frequency capacitance vs voltage curves on N-type MNOS capacitor

6.5.2 The role of surface states and nitride charges

The capacitance-voltage shift due to surface states charges is functions of surface potential ψ_s and charge polarity. From the shape of the HFCV curves, it has been reported [71-75, 95] that surface states in the upper half of the bandgap are acceptor type, while those in the lower half of the bandgap are donor type for both N- and P-type silicon MOS devices. Only negatively charged acceptor states between E_F and the midgap, E_i, contribute to the negative shift in the C-V curve. Gray and Brown [71] claimed that the number of states in the lower half bandgap always equals the number of states in the upper half bandgap. This symmetric property of interface state distribution across the two half bands with respect to the silicon's forbidden band suggests that these are states perturbed from the nearly intrinsic silicon bands. Thus, the total charge at the interface states due to both donors and acceptors is

$$Q_{ss} = q \int_{E_v}^{E_c} [N_{SD}^{+}(E) f_{SD}(E) - N_{SA}^{-}(E) f_{SA}(E)] dE \qquad (6.17)$$

where N_{SD}^{+} and N_{SD}^{-} are the donor-type and acceptor-type interface state densities, respectively; q is the electron charge, and E is the energy integration variable at the Si-SiO_2 interface. The functions $f_{SD}(E)$ and $f_{SA}(E)$ are the donor and acceptor distribution functions given by

$$f_{SD}(E) = \{ 1 + 1/2 \times \exp [(E_F - E_D)/kT] \}^{-1} \quad (6.18)$$

and

$$f_{SA}(E) = \{ 1 + 1/4 \times \exp [(E_A - E_F)/kT] \}^{-1} \quad (6.19)$$

As a first approximation, $f_{SD}(E)$ and $f_{SA}(E)$ can be assumed as a step function with

$$\begin{aligned} f_{SD}(E) &= 0, \quad E_D < E_F \\ &= 1, \quad E_D \geq E_F \end{aligned} \quad (6.20)$$

and

$$\begin{aligned} f_{SA}(E) &= 1, \quad E_A \leq E_F \\ &= 0, \quad E_A > E_F \end{aligned} \quad (6.21)$$

Therefore, Equation (6.17) can be expressed as

$$Q_{ss} \approx q \left[\int_{E_f}^{E_c} N_{SD}^{+}(E)dE - \int_{E_V}^{E_F} N_{SA}^{-}(E)dE \right] \quad (6.22)$$

When a voltage is applied, the interface states move up and down with the valence and conduction band edges while the Fermi level remains fixed. Since donor type N_{SD}^{+} is found in the lower half bandgap, and acceptor type N_{SA}^{-} is

located in the upper half bandgap, Q_{ss} becomes a function of surface potential ψ_s. For an N-substrate MNOS capacitor, in the accumulation region ($\psi_s > \emptyset$) and depletion region ($\emptyset > \psi_s > -\psi_B$), the Q_{ss} is given by

$$Q_{ss}(\psi_s) = -q \int_{E_i(\psi_s)}^{E_F} N_{SA}^{-}(E)dE$$

$$= -q \int_{E_i(\psi_s)}^{E_F} N_{ss}(E)dE \qquad (6.23)$$

and in the inversion region ($\psi_s < -\psi_B$)

$$Q_{ss}(\psi_s) = q \int_{E_F}^{E_i(\psi_s)} N_{SD}^{+}(E)dE$$

$$= q \int_{E_F}^{E_i(\psi_s)} N_{ss}(E)dE \qquad (6.24)$$

where $N_{ss}(E)$ is the surface state densities.

The nitride charge Q_N plays an important role[42] in the switching behavior of an MNOS structure. The study of the relationship between stored nitride charge and the charge distribution in MNOS structures allows better

understanding of trapping properties and retention bahavior of these devices. Charge-centroid concept was introduced in early studies [96-99] which is based on the Poole-Frenkel detrapping mechanism to interpret the propagation of nitride charge towards the metal gate. Arnett [96] described the charge distribution in Si_3N_4 layer during charge trapping. The redistribution of Q_N is caused by the increase of injected charge by appling constant voltage or constant current pulse to the metal gate. Lehovec [97] and Lehovec and Fedotowsky [98-99] described the charge-centroid relation for pronounced Poole-Frenkel detrapping in the nitride using staircase charging method. In short, the charge-centroid relation is

$$X_o = T_N - \frac{\epsilon_n \Delta V_{FB}}{\Delta Q_N} \tag{6.25}$$

where T_N is the nitride thickness; ΔV_{FB} is the flatband voltage shift, and ΔQ_N is the change of nitride charge.

In order to obtain a better understanding of endurance and retention characteristics on nonvolatile MNOS memory devices, the interface states effect (at $Si-SiO_2$) should be carefully studied. The high density of interface states, and the tunneling ability through thin oxide will greatly affect the threshold voltage shift, switching behavior, and charge loss rate. These are the key parameters which determine the performance characteristics of an MNOS device.

In order to quantitatively study the interface states effect on device degradation, we first treat nitride charge as an effective parameter Q_{Neff} and then describe the charge behavior in Si_3N_4 layer or at SiO_2-Si_3N_4 interface based on the data analyzed.

6.5.3 Threshold voltage shift and mobility degradation on the exercised MNOS capacitor

The gate voltage V_g on an N-type MNOS capacitor can be expressed as

$$V_g(\psi_s) = \phi_{ms} + \psi_s - \frac{Q_{ss}(\psi_s) + Q_{sc}(\psi_s)}{C_I} - \frac{Q_{iN} + \int_0^{T_N} \rho(x)\left(1 - \frac{x}{T_N}\right)dx}{C_N} \tag{6.26}$$

where ϕ_{ms} is the work function between metal gate and silicon substrate; ψ_s is the surface potential; $Q_{ss}(\psi_s)$ is the surface state charges per unit area; Q_{in} is the charge stored at SiO_2-Si_3N_4 interface per unit area; $\rho(x)$ is the charge density in Si_3N_4 layer; T_N is the nitride thickness; C_I is the total insulating capacitance per unit area, and C_N is the nitride layer capacitance per unit area. Now, we can define Q_{Neff} as

$$Q_{Neff} \triangleq Q_{iN} + \int_0^{T_N} \rho(x)\left(1 - \frac{x}{T_N}\right)dx \tag{6.27}$$

and Equation (6.26) becomes

$$V_g(\psi_s) = \phi_{ms} + \psi_s - \frac{Q_{ss}(\psi_s) + Q_{sc}(\psi_s)}{C_I} - \frac{Q_{Neff}}{C_N} \qquad (6.28)$$

In Equation (6.28), fixed oxide charge Q_f is neglected due to high surface state density in the MNOS structure. In order to verify the effect of surface states on gate voltage, Q_{Neff} is assumed to be zero for the time being. Rewrite Equation (6.28) as

$$V_g(\psi_s) = \phi_{ms} + \psi_s - \frac{Q_{ss}(\psi_s) + Q_{sc}(\psi_s)}{C_I} \qquad (6.29)$$

The theoretical HFCV curves are calculated for different frequencies ranging from 100KHz to 100MHz for an unexercised P^+-base gridded MNOS capacitor from 1410 mask series. The results are shown in Figure 6.9, where 800 ohms sheet resistance was assumed in the calculation, C_{FB} is at V_g=-0.094 volt, the shift due to Q_{ss} is -0.20 volt, and C_{min} is at V_g=-1.23 volts for 1MHz case. The frequency-dependent capacitance in both the accumulation and depletion regions is due to sheet resistance effect, and in the inversion region it is mainly due to the minority carrier (hole) transport response ability.

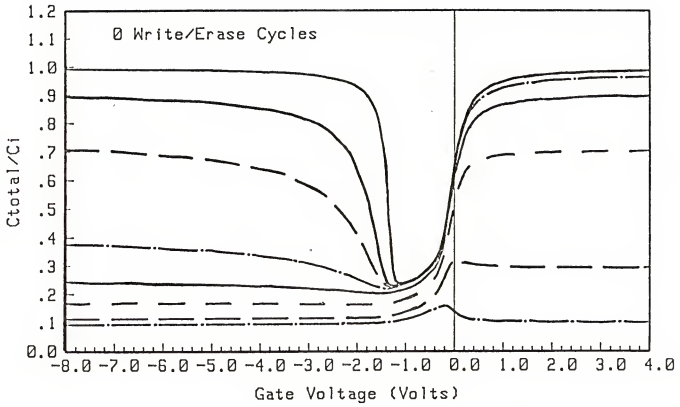


Figure 6.9 The theoretic HFCV for a P^{+}-base MNOS capacitor

Figure 6.10 shows the C-V curves for the P^+-base gridded MNOS capacitors for frequencies of 1, 2, 5, 10, 20, 50 and 100 MHz with gate voltage vary from 0 to -6 volts. In low gate bias region (V_g<-4V), the C-V scan is not affected by charges in the nitride, and the capacitor is known as in its original state. A comparison between the theoretic and the experimental HFCV curves (e.g., 1MHz curve in original state) provides information concerning the original nitride charge density, the Value of which is about $2x10^{12}$ cm^{-2}. Again, by using Equation (6.28), the theoretical HFCV curves are drawn in Figure 6.11. Excellent prediction of P^+-gridded MNOS capacitor is illustrated by equivalent circuit. The small difference of C_{min} between two results is attributed to the extra insulating capacitance of long extended pads of metal contact out of the MNOS capacitor area. This effect is trivial.

The relationship between surface potential and gate voltage for a nonexercised MNOS capacitor with P^+-base grids is shown in Figure 6.12. The dashed line is for an ideal MNOS capacitor with no memory charge into original state. The solid line is for the case when Q_{Neff}/q is $2x10^{12}$ cm^{-2}. The ψ_s vs V_g curves for three different W/E cycles are shown in Figure 6.13. Apparently, the ψ_s vs V_g relation is a function of surface states. In this figure, we can see that when W/E cycle is increased, the curve tends to stretch out with decreasing slope due to the

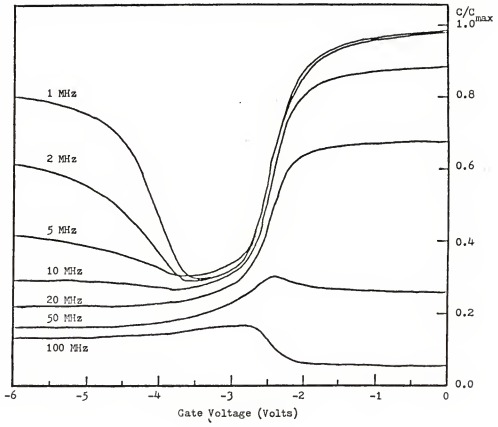


Figure 6.10 The measured high-frequency C-V curves on a P^+-base gridded MNOS capacitor

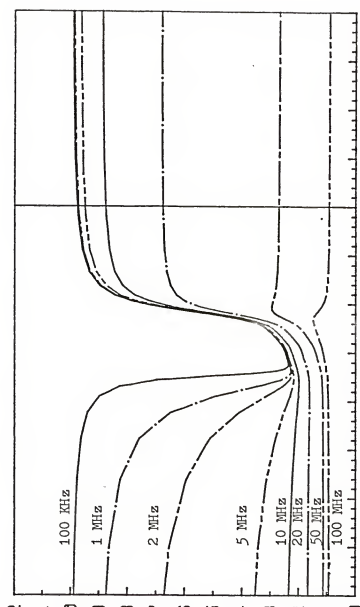


Figure 6.11 The theoretic high frequency C-V curves for a P^+-base grided MNOS capacitor, where grid spacing is 75 μm, grid width is 5 μm, nitride effective charge density is 2×10^{12} cm^{-2}

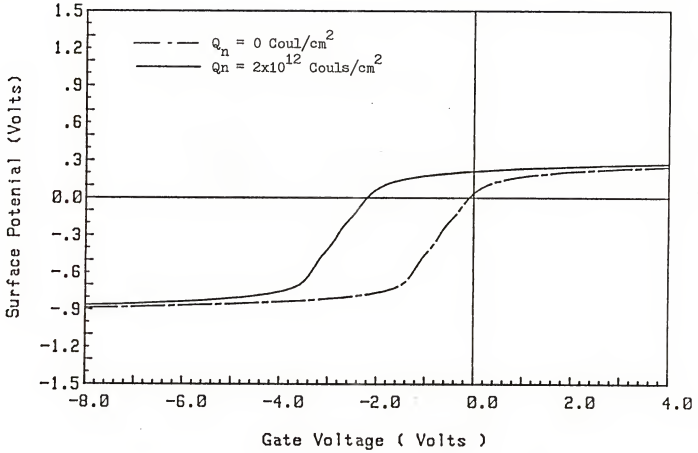


Figure 6.12 A demonstration of the relationship between V_g and surface potential on nonexercised P^+-base MNOS capacitor

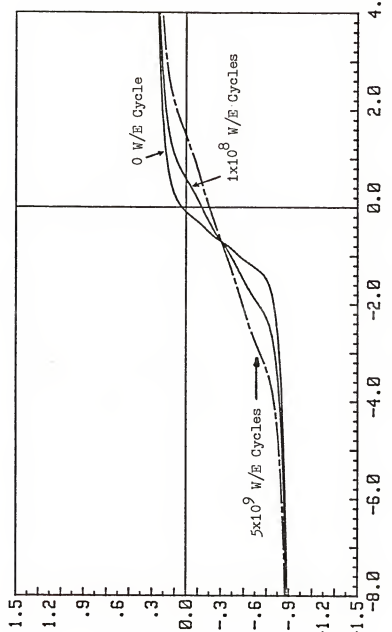


Figure 6.13 An illustration of V_g-surface potential relation for three different exercise conditions

generation of surface state densities. In addition to the surface state dependence, the quantity of memory charge also affects the ψ_s vs V_g relation. Thus, the two factors reduce the accuracy in determining energy distribution and capture cross section of interface states on an MNOS device by employing the admittance method [16].

Figure 6.14 shows the highly distorted HFCV curves taken after W/E cycles of $1x10^9$, and $5x10^9$. The C-V shift is a result of the generation of fast surface states by prolonged W/E cycling. Since all the data taken were in its original states, we assume no shift due to Q_{Neff}. Based on the result in Figure 5.12, three 1MHz C-V curves are calculated and the results are shown in Figure 6.15. A positive shift of C-V curves is due to an increase in acceptor-type surface state densities, and a negative shift is due to an increase in donor-type surface state densities.

A similar C-V distortion phenomenon on the right half curve is presented in both Figure 6.14 and 6.15. Nevertheless, in the inversion region, the negative shift after each W/E cycling has the same amount as in accumulation or in depletion region. We only see the broadening of "U" shape theoretically; no flattening out of C-V curves in the inversion region can be predicted from the contribution of increased surface state charges. The question is therefore raised as to what mechanism causes the flattening out of C-V curves on an actual MNOS capacitor.

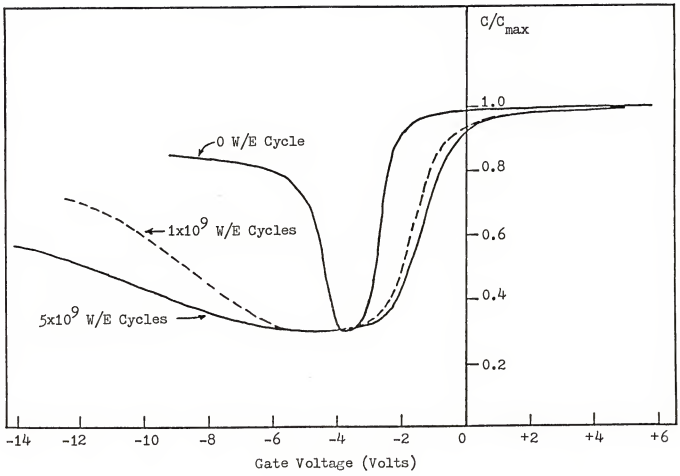


Figure 6.14 A comparison of three C-V curves with three different W/E cycles

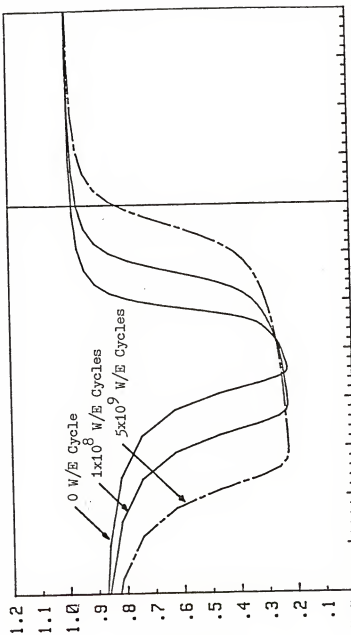


Figure 6.15 The theoretic calculations of the HFCV curves after CC-DLTS measurements

The amplitude of C_{total}/C_I in inversion region depends on the amount of minority carriers (holes in this case) which follows ac high frequencies applied on the gate. It is related to the channel capacitance, channel conductance, and the resistivity of the P^+-grids. Reduction of C_{total}/C_I causes flattening on the left side of the C-V curve. By examining these three parameters, a decrease of channel conductance is possible to explain the reduction of total capacitance. Thus, the degree of channel mobility μ_{eff} reduction is examined and correlated. In Figure 6.16, for a P^+-base gridded MNOS capacitor after $5x10^9$ W/E exercise test, μ_{eff} merely reduces to approximately 30% of the hole mobility for nonexercised device. The mobility may be attributed to the increase in scattering from the interface states plus the effects of vertical electric field E_{eff} and nitride memory charge Q_{Neff}.

To clarify the individual effect on device fatigue phenomena, all data were taken in their original state. This means that no retention loss or no back tunneling current is presented. The threshold voltage shift ΔV_T vs surface potential ψ_s after three memory operations (write/erase) of 0, $1x10^8$, and $5x10^9$ cycles with 26 volts, 10 μs exercised pulses is shown in Figure 6.17. It is assumed that V_T is the threshold voltage when ψ_s is equal to $2\psi_B$. However, in actual MIS transistor modeling, V_T is greater than $2\psi_B$, depending on the definition of turn-on voltage. The threshold voltage shift due to surface state

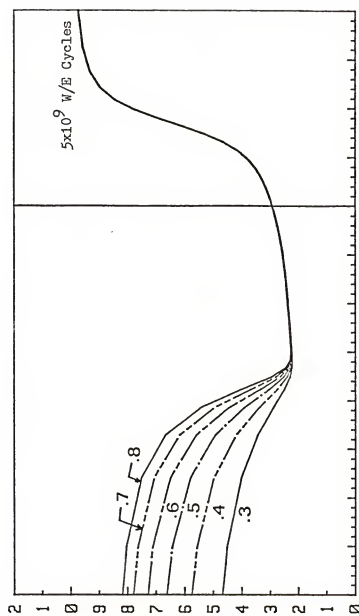


Figure 6.16 The estimation of mobility reduction due to the generation of surface state densities after $5x10^9$ prolonged cycling

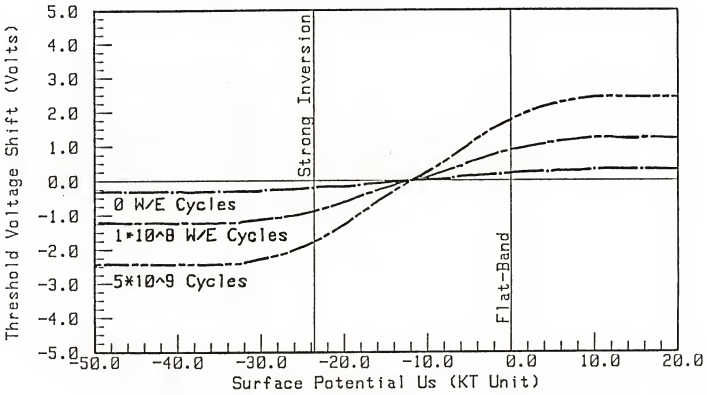


Figure 6.17 The threshold voltage shift vs surface potential with three different prolonged cyclings at 26 volts, 19 μsec pulse

charge is given by

$$\Delta V_T(2\psi_B) = - \frac{\Delta Q_{ss}(2\psi_B)}{C_I} \qquad (6.30)$$

where $Q_{ss}(2\psi_B)$ is definded as the variation of surface state charges between two different exercised cycles. The voltage shifts ΔV_g contributed from surface state charges under three W/E cycles, Ø W/E cycle, $1x10^8$ W/E cycles, and $5x10^9$ W/E cycles are listed in Table 6-1. Combining Figure 6.17 and Table 6-1, ΔV_T can be calculated as a function of the number of cycling. For example, if $\Delta V_T = 2\psi_B$, then, V_T=-Ø.7 volt after $1x10^8$ W/E cycling, and ΔV_T=-1.6 volt after $5x10^9$ W/E cycling. Nevertheless, if the turn-on voltage of an MNOS transistor, ΔV_T, is equal to $2.4\psi_B$ (from computer simulation) then, ΔV_T($1x10^8$ cycles) = -1 volt and ΔV_T($5x10^9$ cycles) = -2 volts, which show a higher threshold voltage shift than that when V_T is egual to $2\psi_B$. The difference is attributed to the different definitions of the turn-on voltage.

In summary, ΔV_T is between -Ø.7 volt and -1.Ø volt for $1x10^8$ W/E cycles and is between -1.6 volts and -2.Ø volts following $5x10^9$ W/E cyclings with 26 volts, 1Ø usec programming pulses. The negative shift of threshold voltage (shown in Figure 3.12) is believed to be due to the increased surface state density at $Si-SiO_2$ interface, which dominates the degradation of endurance.

TABLE 6.1

Mask Series **** 1410 P^+-Base Gridded MNOS Capacitor
Exercised with 26 Volts, 10 μsec pulse
Table of the Threshold Voltage Shift ascribed to the Surface
State Charges after W/E Prolonged Cyclings

Surface Potential (in kT unit)	Q_{st}(0 W/E) (Volts)	Q_{st}(10^8 W/E) (Volts)	Q_{st}(5×10^9 W/E) (Volts)
-34	-.313	-1.230	-2.430
-33	-.308	-1.221	-2.415
-32	-.297	-1.198	-2.380
-31	-.286	-1.173	-2.338
-30	-.275	-1.145	-2.291
-29	-.264	-1.115	-2.236
-28	-.252	-1.081	-2.172
-27	-.241	-1.043	-2.099
-26	-.229	-1.002	-2.015
-25	-.218	-.955	-1.920
-24	-.206	-.904	-1.814
-23	-.194	-.847	-1.699
-22	-.182	-.784	-1.572
-21	-.170	-.714	-1.433
-20	-.158	-.637	-1.281
-19	-.146	-.551	-1.114
-18	-.125	-.459	-.938
-17	-.095	-.370	-.767
-16	-.068	-.285	-.607
-15	-.044	-.204	-.452
-14	-.024	-.128	-.304
-13	-.010	-.055	-.162
-12	-.001	-.006	-.026
-11	.006	.003	.107
-10	.018	.099	.247
- 9	.035	.173	.392
- 8	.058	.252	.544
- 7	.083	.335	.703
- 6	.113	.423	.870
- 5	.141	.514	1.043
- 4	.153	.604	1.216
- 3	.165	.685	1.374
- 2	.177	.757	1.518
- 1	.189	.823	1.650
0	.201	.882	1.770
1	.213	.936	1.879
2	.225	.984	1.978
3	.236	1.027	2.067
4	.248	1.066	2.145

TABLE 6.1 (Continued)

5	.259	1.102	2.211
6	.270	1.134	2.270
7	.282	1.163	2.320
8	.293	1.189	2.364
9	.304	1.212	2.402
10	.313	1.230	2.430

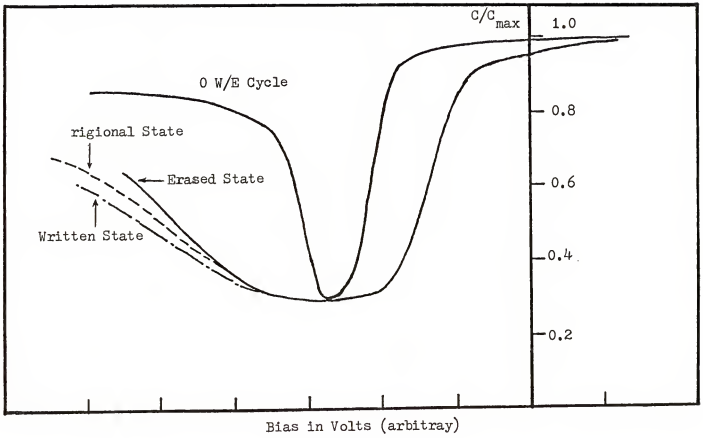


Figure 6.18 An illustration of the nitride charge effect on the mobility degradation in the inversion layer

In contrast to MOS field effect transistor, MNOS devices provide a unique opportunity to vary the nitride charge density without affecting other parameters, so that the inversion layer properties could be studied for a wide range of nitride charge densities on the same device. In this way the role of Coulombic scattering due to charges stored in the nitride could be examined., For instance, if there is a 5 volts negative shift from original state to write state after negative pulse, approximately 4.46×10^{12} cm^{-2} positive (holes) charge density will be injected into nitride through SiO_2 layer. If a 3 volts positively shift from the original state to the erase state after a positive pulse is applied, then there will be about 2.67×10^{12} cm^{-2} electron charge density stored in the nitride. Inspite of the polarity of charges, there will be about the same amount of surface state charges. To examine the nitride charge effect on inversion layer mobility, the C-V curves for write, erase, and origional states after 1×10^{9} W/F cyclings are plotted together in arbitrary voltage scale in Figure 6.18. The mobility degradation due to nitride charges isolated by a thin oxide layer is much less than the influence from the drastic increase of surface state densities after prolonged cycling (i.e. 1×10^{9} W/E cycles).

A gridded capacitor fabricated in 1338 mask series was exercised with o, 1×10^{8}, 6×10^{9}, 3.07×10^{10}, and 1×10^{11} W/E cycles using 28 Volts, 1 sec pulse. The HFCV data were

taken after each W/E cycles and plotted in Figure 6.19. The broadening and flattening of "U" shapes in HFCV curves with increasing W/E cyclings from Ø cycle to $3.07x1Ø^{1Ø}$ cycles are observed. These phenomena reveal the generation of surface state densities in this MNOS capacitor. After $3.Ø7x1Ø^{1Ø}$ W/E cycles, the HFCV curves presented gradual declining in the strong accumulation region as well as shrinking of "U" shapes. The declining of accmulation capacitance implies that oxide layer is no more a good insulating layer as before and becomes conductive. Thus, in addition to the displacement current due to a.c. signal on the gate, there exists leaky current across the thin oxide layer. The shrinking of "U" shape is proposed as a result of the interaction of charges among nitride interface, surface states, and silicon conduction band. As a consequence, the quasi-fermi level posseses a gradient from the surface to silicon bulk, the charged surface states is then less compared with the case of flat quasi-fermi level in the identical surface band bending condition. Therefore, the HFCV curve shrinks in the shape, and the threshold voltage V_T shifts more positively after $3x1Ø^{1Ø}$ W/E cycles.

6.6 Conclusions and Discussion

To meet the need of programming ability for the MNOS capacitor, a fine P-type grided pattern was diffused into the surface of N-type substrate before formation of the MNOS dielectric layers. This provides the required

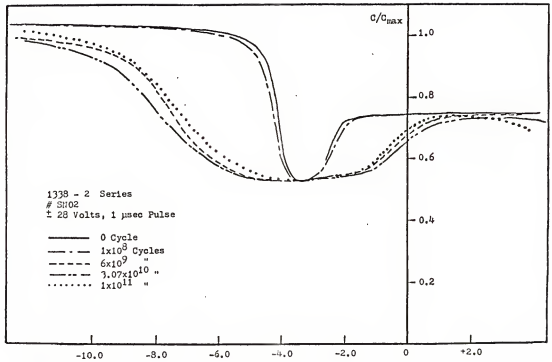


Figure 6.19 The HFCV curves with five different W/E prolonged cyclings

minority carriers for negative stress programming on an MNOS capacitor instead of using an MNOS transistor. It also allows programming times in the order of a few microseconds, thus presenting the possibility of doing endurance test on capacitors as a process control in addition to the pulse CV measurement. An equivalent RC curcuit is developed for characterizing the HFCV behaviors of a P^+-gridded MNOS capacitor.

The HFCV traces exhibit quasi-static phenomenon. This phenomenon resulted in a "U" shape in the C-V plot. The width of the "U" was related to the physical characteristics of the $Si-SiO_2$ interface states. The theoretical C-V curves are consistent with the measured data combining surface state densities using the CC-DLTS technique. The generation of surface state densities results from the high electric stress operations on the MNOS devices. Before 3.07×10^{10} W/E cycles, the width of "U" shape was broadened, and all of the traces had shifted towards more positive flatband voltage while the threshold voltage was shifted negatively. After 3.07×10^{10} W/E cycles, the width of "U" shape started to decrease, while the threshold voltage was shifted backward (positively in N-type MNOS devices), and the decining of accumulation capacitance was observed. These phenomena are proposed due to increased high interface state densities at $Si-SiO_2$ interface which is the origion of the leaky thin oxide layer. A quantitative correlation of the threshold voltage

shift to the generation of surface state density was accomplished in this work.

The gate voltage-surface potential relation was established with respect to the surface state charges after each W/E programming. The reduction of effective mobility in the inversion layer is ascribed to large surface state charges which is thought to be attributed to Coulombic scattering. After $5x10^9$ W/E cycling, the effective clannel mobility is reduced to about 30% of the original value.

From the C-V measurement of the original state, the nitride-oxide interface possesses positive charge with the charge density of about $2x10^{12}$ cm^{-2}. Mobility degradation due to nitride charge has been observed. However, it is not significant compared with the influence arised from large increase in surface state charges at the $Si-SiO_2$ interface after prolonged exercise.

CHAPTER VII
SUMMARY AND CONCLUSIONS

A study of interface states and its correlation to the failure mechanisms of the silicon MNOS nonvolatile memory device has been carried out in this dissertation for different device geometrical structures, device parameters, and exercised conditions. The results show that interface states at the $Si-SiO_2$ interface are the dominant factor causing degradation of endurance and retention of an MNOS device. The CC-DLTS technique has been employed for the first time to characterize the fast surface states at $Si-SiO_2$ interface of MNOS devices. The existing theory for the CC-DLTS technique has been modified to calculate the surface state densities, energy distribution, and electron capture cross sections in the upper half bandgap of silicon. This technique provides the ability to distinguish the fast surface states from the slow states in thin oxide layer and from the memory charge stored in the nitride layer.

The surface state densities for an unexercised MNOS capacitor were found in the range of 2.0×10^{10} to 1×10^{12} $cm^{-2} eV^{-1}$ which is an order of magnitude higher than those of silicon MOS devices fabricated under identical processing

condition. It is ascribed to the penetration of nitride atom through the thin oxide layer to the silicon surface. The electron capture cross sections for the interface states are found to be energy- and temperature-dependent. This result is in contrast to the energy-dependent theory reported by Wang [23] and the temperature-dependent theory proposed by Johnson et al. [26]. Values of measured electron capture cross sections are found to vary from $3x10^{-16}$ cm^2 to $3x10^{-18}$ cm^2, which indicates that the interface traps in the upper half bandgap are of neutral acceptor type. Our CC-DLTS results further reveal that electron capturing by the interface states is via multiphonon process with an activation energy of 36 meV.

The experimental results show that there is little change in the interface state density for W/E cycles less than $1x10^7$ and increase rapidly for W/E cycles greater than $1x10^7$. The results further show that for W/E cycling exceeding $5x10^9$, the interface state density was found to increase slowly with increasing W/E cycles. The negative shift of the threshold voltage in the exercised MNOS capacitor can be attributed to the increase in the density of interface states with W/E cycling. After $3x10^{10}$ W/E cycles, the leakage of thin oxide layer was observed, and it became significant after $1x10^{11}$ prolonged cycles. It is proposed that the leaky oxide condition is the origion of the positively shift of the threshold voltage exceeding $1x10^{11}$ cycles in the endurance plot (see Figure 3.10). The

increase of interface state densities and the degradation of the thin oxide layer after prolonged W/E cycling are responsible for the increas of back tunneling current, which is the origin of retention loss.

The P^+-gridded MNOS capacitor structures are used for characterizing the interface states after each W/E programming. An equivalent circuit model for this gridded structure has been developed to predict the C-V behavior as functions of frequency, interface state density, inversion layer mobility, and the series resistance in the exercised P^+-gridded MNOS capacitors. Good agreement between the calculated and measured capacitance was obtained in this work.

Significant mobility reduction in the inversion layer was observed after prolonged W/E cyclings, which is ascribed to the Coulombic scattering effect. The stored nitride charges on the mobility degradation were found to have less influence than the high surface state densities.

By altering the NH_3/SiH_4 ratio , oxide thickness, and hydrogen annealing conditions, one may improve the endurance and retention characteristics of MNOS devices. Thus, it is suggested that for the studies of the effects of varying the processing parameters as well as device structure parameters on the performance of MNOS device should be pursued in the future. The use of CC-DLTS technique for such a study should prove to be a viable approach for analyzing the degradation mechanisms in the MNOS device.

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